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INTEGRATED INLINE CHARACTERISATION TECHNIQUES FOR IMPROVED SILICON HETEROJUNCTION SOLAR CELL PRODUCTION

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ABSTRACT: Silicon heterojunction (SHJ) technology is gaining market share in photovoltaics due to its lean process sequence, high efficiency potential and low CO_2 footprint. Margins for improvement in performance, yield and cost are decreasing, while at the same time the benefit of even small gains is growing with production volume. It is therefore worthwhile to implement detailed monitoring of process parameters as well as inline characterisation of the cell precursors during production. In this contribution, we present an overview of inline characterisation techniques that are relevant to SHJ cell production and critically discuss their benefits and weaknesses with the help of some showcase examples. We find that inline characterisation is useful at multiple stages of production. Measurements between processing steps allow early detection of defective wafers, preventing unnecessary processing. They also permit evaluation of the performance of individual manufacturing processes. As one prominent example, we demonstrate the generation of highly-resolved thickness maps of the amorphous silicon and transparent conducting oxide layers using reflection spectroscopy combined with multispectral imaging, as well as physical and machine learning models. This method provides information at an unprecedented level of detail about the layer deposition processes that are at the heart of SHJ technology.
Keywords: inline characterisation, silicon heterojunction, SHJ, HJT, silicon solar cells

1 INTRODUCTION

Inline characterisation during the production of silicon heterojunction (SHJ) solar cells offers great advantages for the manufacturer. Testing the finished cells under operating conditions is essential in order to discard defective ones and sort the rest for tiered pricing and optimal module integration. However, characterisation at earlier stages in the production line is beneficial, too. Inspecting the incoming raw wafers allows defective wafers to be rejected, thus saving unnecessary production costs. Cost analysis simulations with SCost [1] predict that if a theoretical portion of 1% of wafers is correctly identified as defective and extracted before metallisation, 20 €ct/kWp are saved. If a critical defect is detected even before deposition of the transparent conductive oxide (TCO), which contains expensive indium, a further 5 €ct/kWp is saved. For an annual production of 1GWp, this equates to savings of 250 k€.

Inline characterisation can further assist in process monitoring and fine-tuned prediction of final cell performance. In this work, we show as examples how an inhomogeneity in the chemical composition of the texturing bath can be detected by spectral reflectometry even before it becomes critical for final cell efficiency. The predictive strength of carrier lifetime measurements after double-sided amorphous silicon deposition, on the other hand, is demonstrated by a good correlation with the final cells' open circuit voltage.

By combining different tools with sophisticated analysis software and machine learning, a detailed picture of the critical attributes of SHJ precursors can be formed. As a prime example, we present an overview over our developed methods for high-resolution thickness mapping of the amorphous silicon (a-Si) and TCO layers based on reflection spectroscopy and multispectral imaging, as well as optical modelling and machine learning. By associating these data with the positions of the wafers in the deposition trays, we obtain a detailed map of the deposition inhomogeneity within the coating machine.

While literature is available on individual characterisation methods, there is little that gives a comprehensive overview of which methods are relevant to the SHJ production line and how they complement each other. Based on our experience in inline inspection along the whole cell manufacturing process and our close collaboration with both in-house SHJ production and industry partners, we evaluated a number of dedicated tools and methods ranging from established standards to novel approaches. Our findings can aid (i) SHJ cell manufacturers in deciding which tools could best improve their production, and (ii) metrology suppliers in identifying wafer quality parameters that are worth measuring and where there is potential for further improvement of inline characterisation technology. The paper aims at bridging the gap between highly technical research papers on the topic and superficial reviews, targeting readers within the PV community but who are not necessarily familiar with either SHJ technology, cell manufacturing or inline characterisation.

2 SIMPLIFIED DESCRIPTION OF THE MANUFACTURING PROCESS FOR SHJ SOLAR CELLS

Figure 1 shows the structure and processing sequence of a silicon heterojunction (SHJ) cell. The as-cut wafers

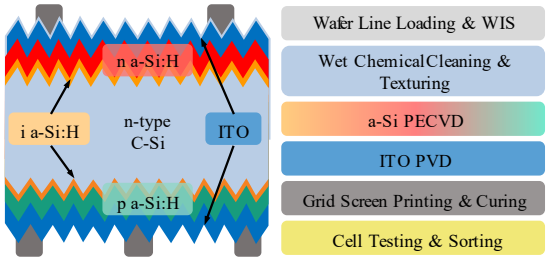

Figure 1: Schematic structure and processing sequence of a SHJ solar cell

are textured on both sides in a series of wet-chemical baths. To passivate the surfaces and to form the junction for carrier separation, differently doped amorphous silicon (a-Si) layers are then deposited on both sides of the wafers in a sequence of plasma-enhanced chemical vapor depositions (PECVD). As a final step in frontend processing, indium-doped tin oxide (ITO) is deposited on both sides via physical vapor deposition (PVD) and forms transparent conductive (TCO) layers, which encapsulate the sensitive a-Si layers and facilitate lateral carrier transport to the contact grid.

In backend processing, the front and back side grids are screen-printed. The wafers are then cured to solidify the paste and allow it to bond to the underlying surface. Finally, the full cells may optionally be laser-cut into half cells or even narrower shingle cells.

3 OVERVIEW OF INLINE CHARACTERISATION METHODS

3.1 The finished cell

The most important inline characterisation step is measuring the electrical performance of the finished cells under standard operating conditions (25°C, 1000 W/m^2, AM1.5G spectrum). Based on the conversion efficiency η or current at the maximum power point I_{MPP}, the cells are binned into quality classes for module integration and sorted out in case of severe defects.

To provide deeper insight into the potential origin of reduced cell efficiencies, spatially- resolved cell inspection techniques have to be added. For instance, electroluminescence (EL) and photoluminescence (PL) imaging not only provide detailed maps of local carrier lifetime; they can also be compared to separate the effects of electrical and optical injection from measured local excess carrier density. The line resistance of the grid fingers can be isolated via grid-resistance neglecting contacting. For bifacial cells, rear illumination and / or using chucks of different reflectivity can emulate the influence of different types of module integration.

3.2 The as-cut wafer

Some unnecessary processing can already be spared, however, by testing the as-cut wafers before they enter the production line to sort out wafers with damage from prior transport and handling. Such incoming wafer inspection may also include measurements associated with the outgoing quality control of the wafer fabrication line. These highly resolved data can help to quantify the influence of the raw material on final cell performance. The simulation in Figure 2 shows the predicted impact of bulk resistivity and lifetime on the final efficiency of SHJ cells. While resistivity can be measured on the as-cut wafer, obtaining accurate bulk lifetime measurements requires passivation of the surfaces. This is already achieved after PECVD of the a-Si layers, though, which is comparatively early in the production sequence. As such, wafers with low lifetime can be sorted out before the deposition of expensive ITO and silver-containing metallisation. This is unique to the SHJ architecture – others, such as PERC or TOPCon, require a late-stage diffusion step that precludes prior knowledge of bulk carrier lifetime. With the impact of the electrical properties shown by the simulation, taking the opportunity to measure them at such early stages provides further cost saving potential compared to other technologies.

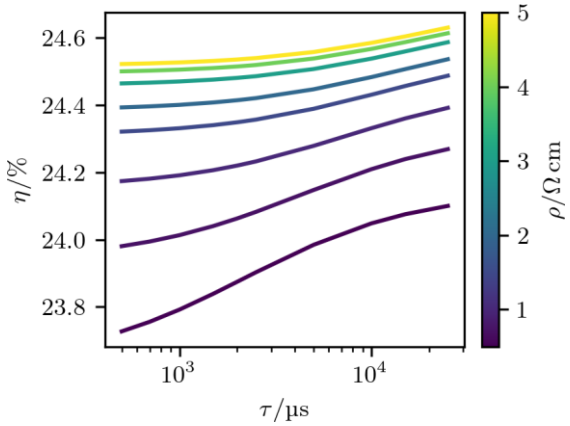

Figure 2: Simulation of efficiency dependence on bulk resistivity and bulk lifetime.

Apart from analysing the bulk material itself, it is equally important to determine the specific mechanical properties of the wafers. High-resolution imaging can be used to identify broken wafers and those whose shape and size are not within the required margins. PL and infrared transmission (IR) imaging can localize microcracks that cause charge carrier recombination, reduced carrier transport and potential breakage of the wafer, even at a later stage during production or handling. These methods also identify other localized defects, although with modern high-lifetime monocrystalline silicon, surface recombination is the dominant cause of contrast in PL images of non-passivated wafers.

Wafer thickness and the extent of saw marks can be measured via laser triangulation or capacitive distance sensors. Wafers that are too thin can result in too low absorption or breakage, while thick wafers may exhibit reduced charge extraction.

3.3 Characterisation after texturing

The quality of the individual processing steps can be assessed by incorporating characterisation in between the steps and ideally evaluating anomalies in terms of their impact on final cell efficiency. The first stage to do this would be after the wet chemical cleaning and texturing steps. Here, care must be taken to reduce the wafers' time spent exposed to the atmosphere, in order to minimize

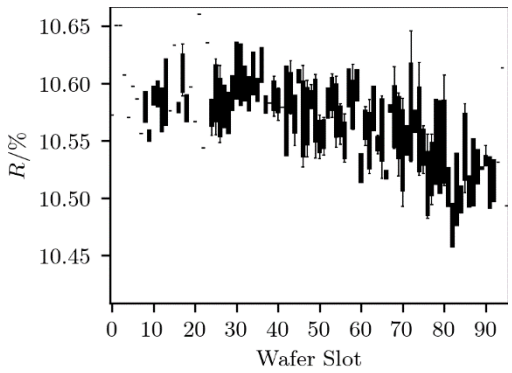

Figure 3: Reflection intensity at 600 nm after texturing. Each box-and-whiskers shows the reflectance distribution of all the wafers in that slot in the carrier. As the carrier lies horizontally in the texturing bath, the slot numbers also correspond to positions across the bath.

oxidation of the bare silicon. Hence, integration of the characterisation equipment into the existing automated production line is critical.

Figure 3 shows a gradient in mean reflection at 600nm against the position of wafers in the wet chemical baths. These wafers were a subset of the same batch of precursors mentioned in Section 3.1. No deliberate variation of texturing conditions was intended. Nevertheless, this gradient indicates slightly inhomogeneous etching of the surface texture across the length of the bath. In fact, OPAL2 simulations show that an increase in reflection intensity can be a direct result of increased planar fraction (Figure 4, blue).

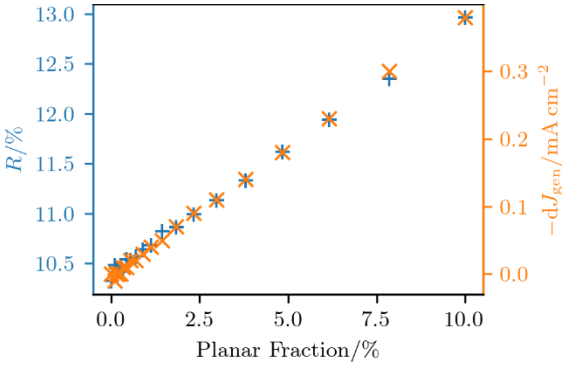

Figure 4: Simulated impact of the planar fraction on the reflection intensity at 600 nm (blue) and the resulting loss in photogeneration current (orange).

Furthermore, this is predicted to have a proportional detrimental effect on the photogeneration current of the finished solar cell (Figure 4, orange). However, comparing the scales on the Y axes of Figure 4 with that of Figure 3, it is clear that no significant loss of performance is to be expected from the small variation in the constitution of the chemical bath observed in this production. This means, on the other hand, that reflection measurements after texturing are very sensitive towards texture quality and can serve as an early warning system against irregularities in the etching process, well before they significantly affect final cell performance.

This measurement has to be done directly after texturing, however, as after a-Si and TCO deposition the reflection intensity is dominated by the properties of the applied layers and no longer shows a clear trend with surface texture.

3.4 Characterisation after layer deposition

As mentioned in the introduction, intermediate characterisation after TCO coating, i.e. before metallisation, has high potential for cost savings. Furthermore, at this stage, many of the physical properties of the finished cell are already fully defined and measurable without the influence of the grid. Meanwhile, the quality of the surface texture as well as the a-Si and TCO layers can still be evaluated.

Due to the robustness of the precursors after TCO coating compared to earlier stages, handling and exposure to the environment can be tolerated at this point, making it an ideal place for extensive characterisation in our study. In fact, during our recent production of 1500 SHJ cells mentioned above, the wafers were transported back and forth between cities for characterisation between ITO deposition and metallisation. They were stacked with separating paper and packed in plastic at atmospheric pressure. Their median performance showed no significant reduction (see Figure 5). Merely the number of outliers

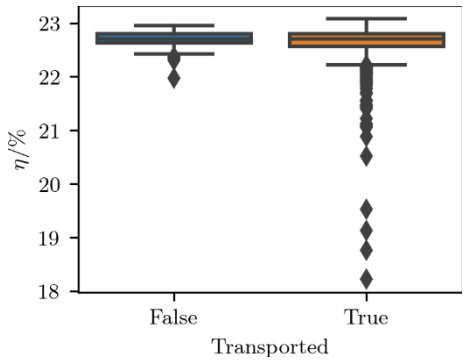

Figure 5: Effect of transport to an off-site frontend wafer inspection system (FWIS) after ITO coating.

increased, which can be attributed to the outer wafers in each package, which experienced increased abrasion.

As surface passivation quality is fully established after TCO, measurements of the effective minority carrier lifetime τ_{eff} are meaningful in terms of cell performance. Figure 6 shows the τ_{eff} values measured by means of the quasi-steady-state photoconductance (QSSPC) technique and plotted against the open-circuit voltage (V_{OC}) for the same batch of SHJ cells as mentioned above. While V_{OC} is recorded on the finished cells, lifetime is measured directly after ITO deposition. As expected, a correlation between

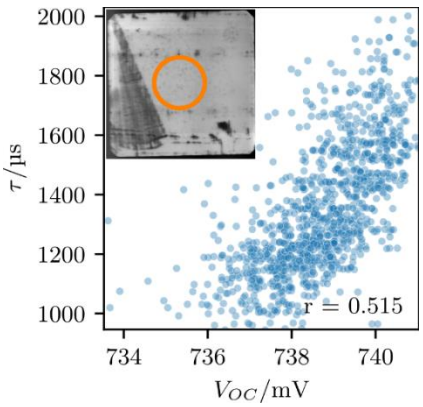

Figure 6: Minority carrier lifetime after PVD vs. open circuit voltage V_{oc} of the finished cell. Inset shows a PL image of a wafer with damage outside the detection area of the QSSPC lifetime tool (orange circle).

τ_{eff} and V_{OC} is visible. However, lateral lifetime inhomogeneities, as seen in the inset PL image, are generally not detected within the central integration area (orange circle) of the QSSPC lifetime tool although they do affect cell performance – this explains the strong scattering observed in Figure 6. To account for these

lateral inhomogeneities, PL images have to be recorded and evaluated with machine learning methods or ELBA analysis [2].

4 LAYER THICKNESS MAPS

The layers deposited onto the silicon wafer via PECVD and PVD are the core features of the heterojunction architecture. The 5-20 nm thick amorphous silicon (a-Si) layers form the carrier-selective layers that enable charge separation after photogeneration, which is the basic functionality of a solar cell [3]. They also passivate the bare silicon surface, reducing recombination. The encapsulating 20-70 nm thick layer of transparent conductive oxide, usually indium-doped tin oxide (ITO), provides lateral transport to the grid, while at the same time allowing light to pass through it as well as protecting the delicate a-Si layers underneath.

Achieving good coverage of these materials with optimal and uniform layer thicknesses is essential for the performance of the solar cell. Too thin an a-Si layer creates not enough of a step in the relevant band, leading to poor charge selectivity. Too thick a layer prevents light from reaching the absorption region; in fact, the parasitic absorption in the a-Si layers reduces the short-circuit current density of the solar cell by 0.16 $mAcm^{-2}$ per nanometre thickness [4]. With ITO, a balance has to be struck between optical transmission and lateral conductivity when choosing the right thickness [5]. Furthermore, the rear-side wafer edge is masked during ITO deposition, in order to prevent wrap-around and consequent short-circuiting of the opposite terminals. An optimal width of the exclusion region must be found to effectively prevent shunts while maximizing the active area of the wafer.

To fine-tune the processing parameters that determine the quality of these critical layers, accurate spatially-resolved thickness maps would be ideal. A precise, non-destructive method of determining thin-film thicknesses is (spectral) ellipsometry. The technique requires precise sample positioning and integration times on the order of minutes for clear results, thus only allowing measurements at individual spots, rather than maps, and not at inline-compatible speeds to date.

4.1 Using a physical model to obtain layer thickness from reflection spectra

An alternative approach uses the thickness dependence of reflection spectra of the layers [6]. Figure 7, for example, shows the variation of the reflection spectrum for different a-Si thicknesses. We have developed a method for determining the thickness based on the reflection spectrum [7]. In this method, an optical model of the layer stack is created, and the Fresnel equations are used to set up a series of transfer matrices, describing the optical transmission and reflection at each interface. With this transfer matrix method (TMM), a simulated reflection spectrum can be generated based on the optical constants and the thicknesses of the constituent layers. The optical constants can be determined once for each given material using ellipsometry, and the layer thickness can be used as a variable to fit the simulated spectrum to a measured one. Such reflection measurements can be carried out with an inline spectrometer, which yields fast and well-calibrated data but is restricted to provide data only along traces [8].

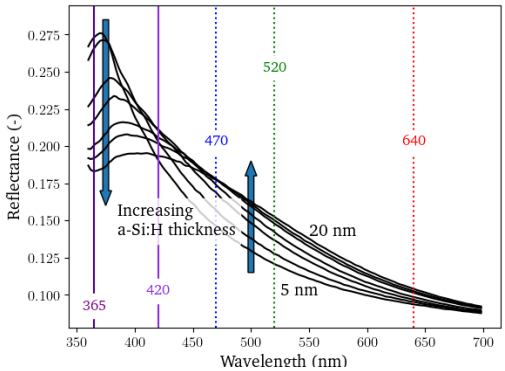

Figure 7: Dependence of the reflection spectrum on a-Si layer thickness. The discrete wavelengths used in multispectral imaging are indicated by the vertical lines.

4.2 Thickness maps from multispectral images

We have further determined that only a few reflection measurements at critical points in the spectrum are sufficient to obtain an accurate fit. For an a-Si layer, a selection of such discrete wavelengths is shown in Figure 7 by the coloured vertical lines. Particularly in the UV (at 365nm) and in the green (520nm), strong variations in reflectance occur with changing layer thickness [6]. For ITO layers, the variation in the red, green and blue channels in the visible spectrum is sufficient.

This enables us to use multispectral imaging to obtain highly resolved reflection data in the wavelengths required for thickness determination. The method works by recording multiple images in quick succession, each illuminated by narrow-band LEDs of different peak wavelengths. The pixel values are calibrated to reflection intensities using a photospectrometer, and all unique combinations of the different wavelength intensities are fitted to thickness values, creating a lookup table. With this table, a detailed thickness map can be computed in minutes.

Figure 8 shows a thickness map of the a-Si layer stack generated by this method [6]. For demonstration purposes, wafer chips were placed onto the sample during the coating process to prevent a-Si deposition in certain patches. They were removed at different times during the

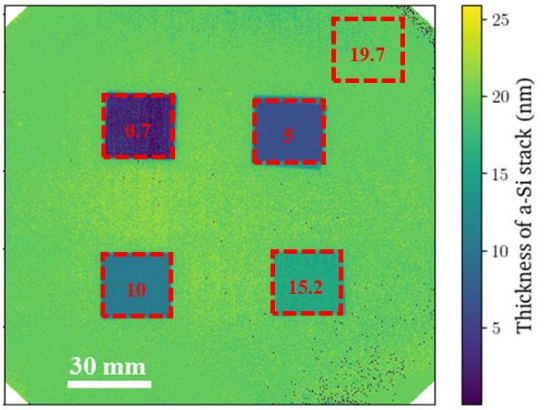

Figure 8: Thickness map of the a-Si stack on a SHJ precursor, determined via inline photospectrometry and multispectral imaging. The dark patches were covered by wafer chips for different durations during PECVD, resulting in different amounts of a-Si deposition in those areas.

process, leading to different coating thicknesses in the four patches. The thickness variation is clearly visible in the image. The top-right patch shows an overlap of two misaligned, partially coated squares. This is due to the covering chip having moved during deposition. The sharpness of the transition between the patches and the surrounding coated area is limited not by the spatial resolution of the measurement but by the vapor creeping in between the sample surface and the covering chips during deposition. Comparisons with ellipsometry data show excellent accuracy of the method [6].

4.3 Fast and robust prediction of thickness maps with machine learning

Taking a few minutes to calculate thickness maps from multispectral images is still not fast enough for real-time inline processing. Furthermore, systematic errors such as those due to inhomogeneous illumination cannot easily be eliminated by some fixed calibration routine, as their magnitude and position with respect to the wafer depend on its positioning within the tool: there is significant coupling between the wafer and the illumination dome, as light bounces between the two multiple times before hitting the camera.

We addressed these issues by developing a machine learning algorithm for fast prediction of layer thicknesses. Our current algorithm has been developed for ITO; a corresponding one for a-Si is in development. The algorithm is based on a physics-informed convolutional neural network, which is trained on synthetic image data with both random and systematic errors added to them. This approach allows a large volume of training data to be used and results in a robust algorithm that is suitable for real-time inline use. It is not only able to create accurate thickness maps of the deposited ITO layer within one second per wafer, but it also accurately and precisely detects the wafer edge and characterises the ITO exclusion region [9].

Such an edge exclusion evaluation is shown in Figure 9, where a detailed map of the ITO thickness gradient is shown for each of the four edges. From this analysis, we can clearly see for this particular example wafer that there are some sections along the top and right edges that are only partially masked. These could lead to shunts. The fine spatial resolution not only reveals unevenness in the mask edge, which causes local fluctuations of the exclusion width, but also a misalignment of the mask, which is visible in this example by the left and bottom edges having a wider average exclusion region than the top and right edges [9].

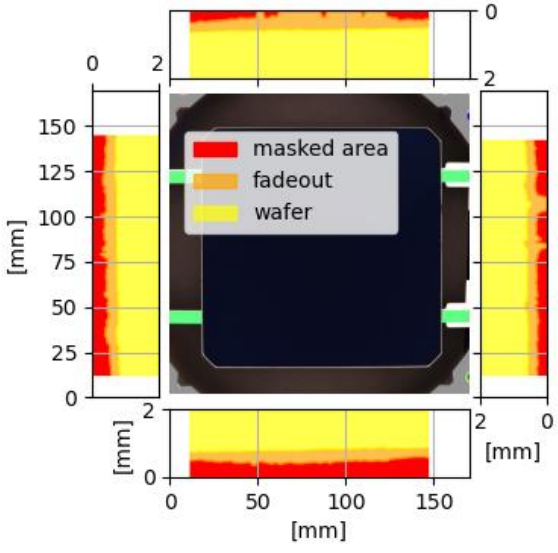

Figure 9: Edge exclusion mapping using multispectral imaging and machine learning.

We used our machine learning algorithm to generate high-resolution thickness maps of the ITO layer on ~900 wafers of the aforementioned experiment. Associating these maps to the positions of the wafers in the PVD chamber can be used qualitatively to monitor the uniformity of the deposition within the chamber. Figure 10 shows the mean thickness map for each position on the deposition tray. Averaging over ~30 maps per position, random inhomogeneities and effects of other processing steps are cancelled out, and localised deposition density is clearly visible.

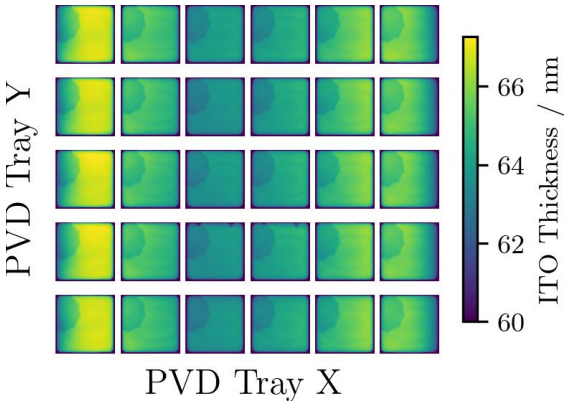

Figure 10: ITO thickness maps vs. position in the deposition tray.

This example shows a clear variation along the X axis. The highest thickness is deposited in two stripes close to the left and right edges of the tray, with minima in the middle of the tray and at the outermost edges. Note that the polygonal shape visible in the top-left corner of each image is a lens artifact of our setup; the problem has since been addressed.

5 OUTLOOK

Modern SHJ cell production has reached levels of reproducibility such that the spread of efficiencies is low, see Figure 11. It is no longer enough to record one statistical datapoint for each wafer with each measurement tool. We have seen for the evaluation of a-Si and TCO layer thicknesses that spatial information is crucial to further improve the characterisation of anomalies. The only significant difference between the left-hand-side and the right-hand-side PL images inset in Figure 11 is the local horizontal dark areas, likely due to damage of an underlying layer. Yet they correspond to wafers on opposite ends of the η distribution, so it is important to identify such defects (and many more subtle ones) automatically.

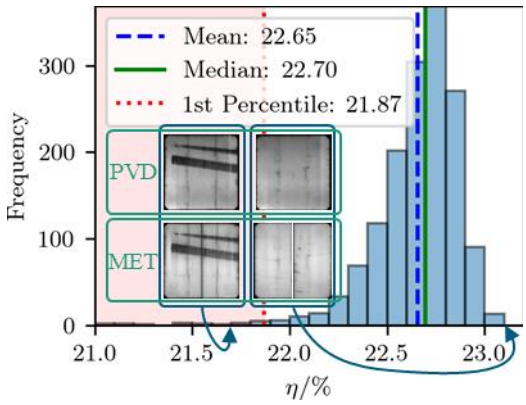

Figure 11: Efficiency distribution for our recent industrial production of SHJ cells. Inset: PL images of a wafer with $\eta = 21.70\,\%$ (left) and one with $\eta = 23.06\,\%$. Top images were recorded after ITO PVD, bottom ones on the finished cells (after metallisation).

Fortunately, we can use machine learning for such tasks, which we have already applied to the layer thickness mapping (Section 4.3), and which we are currently developing further for other characterisation techniques. And such methods have great impact when the defects are visible early in the production sequence. In the example in Figure 11, the top row of images was recorded after PVD of the ITO layer, i.e. before metallisation.

It will require such early measurements of spatialy-resolved precursor parameters combined with sensitive yet robust machine learning algorithms in order to further reduce processing costs by sorting out such wafers, as discussed in the Introduction. The development of such methods is ongoing.

6 CONCLUSION

In conclusion, there are numerous inline characterisation techniques that provide valuable quality assurance and thus enable efficient process development in silicon heterojunction solar cell production. Precision of these techniques is high enough that they are able to resolve the small differences remaining in the quality of cells in modern manufacturing. They can be combined to produce detailed quantitative maps of wafer and cell parameters, and they can help to predict final cell performance early in the production line as well as to monitor and improve individual processes.

7 ACKNOWLEDGEMENTS

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