

TWO-TERMINAL III-V//SI TRIPLE-JUNCTION SOLAR CELL WITH POWER CONVERSION EFFICIENCY OF 35.9 % AT AM1.5G

Patrick Schygulla, Ralph Müller, Oliver Höhn, Hubert Hauser, Benedikt Bläsi, Felix Predan, Jan Benick, Martin Hermle, Frank Dimroth, Stefan W. Glunz, and David Lackner
Fraunhofer Institute for Solar Energy Systems ISE
Heidenhofstr. 2, 79110 Freiburg, Germany

ABSTRACT: III-V//Si multi-junction solar cells offer a pathway to increase the power conversion efficiency beyond the fundamental Auger limit of silicon single-junctions. In this work we demonstrate how the efficiency of a two-terminal wafer-bonded III-V//Si triple-junction solar cell is increased from 34.1 % to 35.9 % under an AM1.5g spectrum, the highest reported efficiency for silicon based multi-junction solar cell technologies. This improvement was accomplished by two main factors. First, the integration of a GaInAsP absorber in the middle cell increased the open-circuit voltage by 51 mV. Second, a better current matching of all subcells enhanced the short-circuit current by 0.7 mA/cm².

Keywords: MOVPE, III-V/Si, silicon based tandem solar cells, multijunction solar cells, GaInAsP, wafer bond

1 INTRODUCTION

Single-junction crystalline silicon solar cells have a theoretical efficiency limit between 29.4 % and 29.5 % [1, 2]. To make better use of limited areas and to continue reducing leveled costs of electricity in terrestrial applications, it is vital to explore new solar cell concepts that can exceed this limit. In multi-junction solar cells thermalisation and non-absorption losses are reduced and thus the efficiency limit is enhanced. The current record efficiency of all solar cell concepts under one-sun AM1.5g illumination was demonstrated for an inverted metamorphic sextuple-junction solar cell and amounted to 39.2 % [3].

Such multi-junction solar cells are based on III-V compound semiconductors. The need of rare elements for wafers and precursors, the expensive facilities that are required for epitaxial growth and cell processing, and the low numbers of produced units result in large cell costs of around 60 \$/W_{DC} [4] which is more than two orders of magnitude larger compared to single-junction silicon (Si) cells. Strong efforts are being undertaken to reduce the cost of III-V solar cell fabrication. One important breakthrough towards this goal are demonstrated growth rates above 120 μm/h [5, 6]. The substrate costs amount to around a third of the total costs for III-V multi-junction solar cells. Substrate removal and reuse approaches can thus also help to reduce these costs [7]. Here, the expensive substrate is used for epitaxial growth and then the solar cell is transferred to a carrier wafer consisting of a cheaper material.

Another possibility is to use a less expensive substrate material, for instance silicon, as the bottom cell of a multi-junction architecture. The III-V cell layer stack can be grown directly on the Si cell using a metamorphic buffer structure [8, 9] to overcome the mismatch in lattice constants between Si and the III-V cells. The highest power conversion efficiency was reported for a triple-junction GaInP/GaAs/Si solar cell with a value of 25.9 % [10]. This cell suffers from a voltage loss due to non-radiative recombination at the threading dislocation defects introduced by the metamorphic buffer growth. This loss mechanism can be avoided if the III-V top structure is grown lattice matched on GaAs and then either mechanically stacked on the Si cell (four-terminal configuration) [11] or monolithically connected to the Si cell (two-terminal configuration). The latter can be

achieved by using either a direct wafer bond [12] or a transparent conductive adhesive [13].

With a four-terminal design the maximum conversion efficiency demonstrated amounted to 35.9 % for a triple-junction GaInP/GaAs-Si solar cell [11]. This has so far been the highest conversion efficiency of any silicon based multi-junction solar cell [14]. The two-terminal configuration allows for a direct integration into modules and the exploitation of existing technology for Si solar panels. The previous wafer bonded triple-junction GaInP/AlGaAs//Si champion device, however, achieved a lower maximum conversion efficiency of 34.1 % [15]. Other promising developments for cost reduction in multi-junction solar cells include the combination of a perovskite/Si dual-junction. This technology has recently obtained a record conversion efficiency of 29.2 % [16].

Hence, combining the high-efficiency multi-junction concept with the mature and cost-effective silicon technology is a promising route for redefining the practical solar cell efficiency limit. In this work, we explore the experimental efficiency potential of monolithic wafer-bonded III-V//Si triple-junction solar cells in a two-terminal configuration.

2 EXPERIMENTAL METHODS

2.1 Solar Cell Design

The ideal band gap combinations of the upper two junctions were calculated to be 2.01 eV and 1.50 eV [17]. For the top junction only AlGaInP or AlGaAs can be grown at the required band gap lattice matched to GaAs. Both exhibit severe disadvantages, though. Al_{0.55}Ga_{0.45}As is an indirect semiconductor and hence unsuitable for maximising the voltage. Al_{0.11}Ga_{0.40}In_{0.49}P is known to have a rather low carrier mobility and an increased incorporation probability for parasitic oxygen resulting in reduced diffusion lengths, reduced open-circuit voltage, and increased sheet resistance, which is detrimental for the uppermost junction [18]. Choosing GaInP with a direct band gap of 1.90 eV our group can at present reach higher absolute voltages in practice. Because of a higher minority carrier lifetime and reduced recombination in the depletion region resulting in higher voltages and a higher filling factor a rear-heterojunction cell architecture with a thin AlGaInP base was implemented [19]. Choosing a lower band gap top junction absorber does not alter the ideal middle cell band gap, though, which

remains at 1.50 eV. This band gap can be realised either by $\text{Al}_{0.06}\text{Ga}_{0.94}\text{As}$ [20] or $\text{Ga}_{0.93}\text{In}_{0.07}\text{As}_{0.87}\text{P}_{0.13}$ [21] as shown in Figure 1.

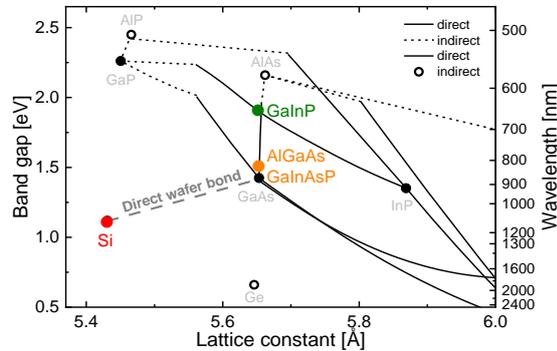


Figure 1. The target band gaps for the top III-V-dual-junction at 1.90 and 1.50 eV can be realised by GaInP and GaInAsP or AlGaAs. To overcome the large lattice mismatch between the III-V semiconductors and silicon a direct wafer bond is used.

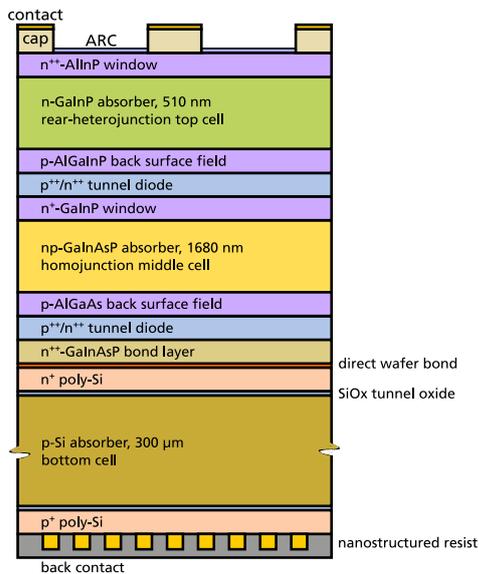


Figure 2. Schematic layer stack of the III-V//Si triple-junction solar cell design including a double-layer antireflection coating (ARC), a highly doped n-GaAs cap layer below the contacts, a GaInP-rear-heterojunction top cell, a GaInAsP homojunction middle cell, a silicon bottom cell with tunnel oxide passivating contacts (TOPCon), and a nanostructured diffractive rear-side grating for light path enhancement.

2.2 Epitaxial Growth of the III-V Top Structure

The III-V top junction solar cells were grown using metalorganic vapor phase epitaxy (MOVPE) in a commercial AIXTRON AIX2800G4-TM reactor. GaAs wafers of 4" size with a 6° miscut of the (001) surface towards the (111)-B direction were employed as substrates. The precursors for the group-III elements were trimethylgallium (TMGa), trimethylindium (TMIn), and trimethylaluminium (TMAI). For the group-V elements phosphine (PH_3) and arsine (AsH_3) were used. The doping agent precursor for n-type absorber layers was silane (SiH_4). For p-type material dimethylzinc (DMZn) was used. Epitaxial growth was performed at

standard growth temperatures ranging from 550 – 680 °C with a preference for lower temperatures where possible to reduce the thermal load and interdiffusion effects. The V/III ratios were set between 20 and 40 for arsenide-based layers and between 60 and 140 for phosphide-based layers. For the top and middle junction absorber layers the V/III-ratio has been optimised in terms of the open-circuit voltage of single-junction component cells [22]. Hydrogen was used as the carrier gas for the precursors.

2.3 Silicon Bottom Cell

Float-zone grown p-type silicon wafers with a bulk resistivity of 4 Ω cm and a thickness of 280 μm, that had been polished on both sides, were used for the fabrication of the silicon bottom cells. Tunnel-oxide passivating contacts (TOPCon) [23] were formed on the n-type front and p-type back side. These layers passivate the surface very well and thus allow for a high voltage. A thin oxide was grown in HNO_3 . A 100 nm thick intrinsic amorphous silicon was deposited by liquid phase chemical vapor deposition (LPCVD) on both sides. This layer was then doped by ion implantation of phosphorus at the front and of boron monofluoride at the back side. The amorphous layer was eventually annealed to polysilicon at 850 °C. Last, the samples were exposed to a remote hydrogen plasma at 425 °C. The front side was polished by chemical mechanical treatment (CMP) to remove particles and thin the poly-Si layer to around half its thickness.

2.4 Solar Cell Processing

The samples were first temporarily bonded to a sapphire carrier wafer. Then, the GaAs substrate was etched away, and the uncovered bond surface was smoothed by chemical mechanical polishing (CMP). Next, a direct wafer bond between the III-V layer stack and the silicon bottom cell was performed in an Ayumi SAB100 high vacuum direct wafer bonder. The native oxides of the surfaces were first removed by argon ion sputtering at an energy of 0.3-0.4 keV. Then, the wafers were pressed together with a force of 2.4 – 10 kN for 5 min. Further details on the wafer bonding process can be found elsewhere [12, 24]. The sapphire carrier wafer was removed by thermal slide at 190 °C.

The front contacts were deposited with the help of photolithography and metal evaporation. The cell area of 4.028 cm² was defined by wet chemical mesa etching. A $\text{Ta}_2\text{O}_5/\text{MgF}_2$ antireflection coating (ARC) was deposited on the front side by evaporation. On the rear side an optical grating for light path enhancement in the silicon cell was implemented by nanoimprint lithography of a SU-8 photo resist [25]. Finally, a 1 μm thick silver contact layer was deposited on the nanostructured grating.

2.5 Solar Cell Characterisation

The triple-junction solar cells were characterised in the Fraunhofer ISE CalLab under calibrated conditions. The external quantum efficiency (EQE) was measured with a grating monochromator and adjustable bias illumination in lock-in mode. Current-voltage (IV) characteristics were acquired for one-sun conditions using the AM1.5g spectrum (IEC90604-3, ed. 2 with 1000 W/m²). A spectrally adjustable sun simulator with one xenon and two halogen lamp fields at a cell temperature of 25 °C was used to set the correct

illumination conditions [26]. For the analysis of the current-voltage data the two-diode model including resistances was employed [27].

Electroluminescence (EL) spectra were acquired under different injection conditions. Applying the reciprocity relations [28], the EQE and EL could be combined to calculate the contribution of each junction to the overall open-circuit voltage as a function of the short-circuit current density [29]. The band gaps of the III-V semiconductors were determined from the intersection of two exponential fits to the EQE [30].

3 RESULTS AND DISCUSSION

3.1 Performance under One-Sun Illumination

The external quantum efficiencies (EQE) of the three subcells of a triple-junction solar cell with upright grown top cell structure and their sum are shown in Figure 3. Integrating the AM1.5g spectrum under consideration of the quantum efficiency of each junction, one obtains the photocurrent beyond which the respective junction becomes limiting. The GaInP top junction is slightly too thick for a perfect current match and the Si bottom cell limits the total current density that is produced by the triple-junction. An additional solar resource of 0.67 mA/cm² or 0.22 mA/cm² per subcell could still be distributed by adjusting the absorber layer thicknesses. Note that the sum of the EQEs is constant at a high level ranging between 95 % and 98 % in the wavelength interval from 470 nm to 910 nm.

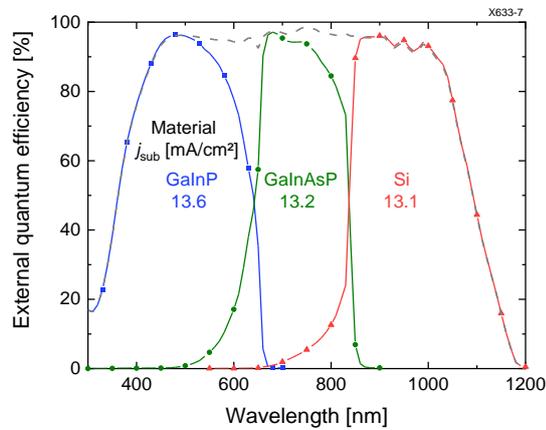


Figure 3. External quantum efficiencies of the top (blue, squares), middle (green, circles), bottom (red, triangles) subcells, and the overall sum (grey, dashed) in the two-terminal record III-V//Si solar cell X633-7. The current density that each subcell could contribute to the photocurrent is given below the absorber material for each junction. The external quantum efficiencies were calibrated using the short-circuit current density of the triple-junction solar cell.

The current-voltage characteristics of the champion cell is presented in Figure 4. Compared to the previous III-V//Si record device [15] with a conversion efficiency of 34.1 % the performance could be improved by 5.3 %_{rel} or 1.8 %_{abs}. The two main reasons for this improvement were an increase in the voltage and in the current density. The open-circuit voltage (V_{oc}) was improved by 2.2 % or 71 mV. The origin of this voltage gain will be discussed in more detail in the following section. The current density could be enhanced by 5 % or 0.7 mA/cm². The

previous cell was strongly current limited by the second junction with an AlGaAs absorber layer with a maximum difference in subcell current of 1.2 mA/cm² [15]. This imbalance could be reduced to 0.6 mA/cm² in the current champion device thanks to an increased quantum efficiency and thus current generation in the GaInAsP based middle junction.

From fitting the IV-curve with a two-diode model the series resistance was found to be around 1 Ω cm². Since the solar cell is designed to work under one-sun condition, this results in a rather low voltage and filling factor loss. The low series resistance is a confirmation of the electrical functionality of the wafer bond and of a sufficiently high conductivity in the n-GaInP top layer. No impact of a finite parallel resistance could be observed in the modelling.

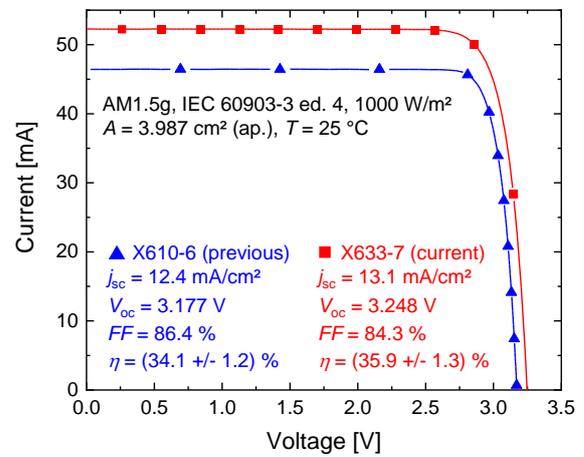


Figure 4. Current-voltage characteristics of the current two-terminal record III-V//Si solar cell X633-7 (red, squares) compared to the previous champion device X610-6 (blue, triangles) under the AM1.5g spectrum.

3.2 Voltage Gain by Improved Subcell Absorber Material

The improvement in open-circuit voltage compared to the previous champion device [15] can be understood from the subcell voltages shown in Figure 5. The voltage increases logarithmically with increasing injection current density because of the higher resulting charge carrier density. At injection conditions that correspond to AM1.5g illumination, 13.1 mA/cm² in this case, the open-circuit voltage can be broken down into a contribution of the three subcells. Comparing these subcell voltages to the ones of the previous champion device X610-6 the improvements can mostly be attributed to one development step. The biggest voltage gain resulted from replacing the AlGaAs absorber by a GaInAsP absorber in the middle junction as shown in Figure 5. As both materials had a similar band gap to within 10 meV, the gain is due to an increased minority carrier lifetime resulting in a lower loss to the radiative limit on substrate of 55 mV, or 125 mV for a cell with perfect rear-side reflector. This corresponds to an external radiative efficiency on substrate of 11.1 %. Given that this is a value of a junction inside a multilayer structure this compares well to the highest performing GaAs single-junction solar cell which has a rear-side mirror and exhibits an external radiative efficiency on mirror of 35.7 % [31]. A second smaller voltage gain originates in the GaInP top cell. Possible reasons for this

increase could be fluctuations in the solar cell processing which damage the top cell most, e.g. from the ARC deposition or cap etching inhomogeneities that generate local shunts.

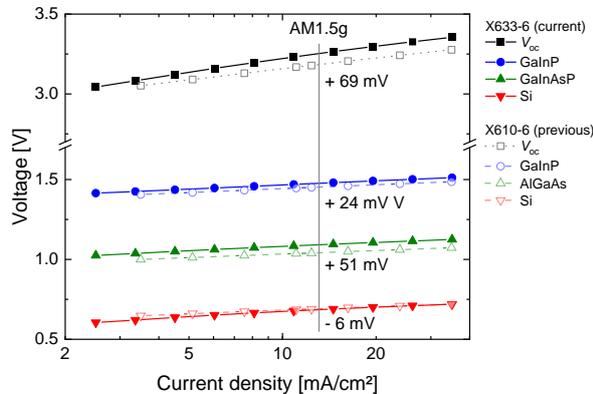


Figure 5. Open-circuit voltages (black, squares) and subcell voltages (coloured, squares, triangles) of the cell X633-6 from the current record III-V//Si wafer (solid, filled symbols) and of the previous champion device X610-6 (dotted, open symbols) at different injection current densities.

4 CONCLUSIONS

We have shown how the efficiency potential of silicon based multi-junction solar cells can be further exploited. By choosing III-V semiconductor materials, that can be deposited with a high crystal quality at the right band gap, and improving the MOVPE growth conditions for these materials we were able to present a two-terminal wafer-bonded triple-junction solar cell which sets a new efficiency record with 35.9 % under an AM1.5g spectrum. In particular, the employment of a GaInAsP middle junction resulted in a significant voltage gain.

It was demonstrated that a monolithic, two-terminal silicon based multi-junction can achieve at least the same efficiency as the currently best performing four-terminal device. No separate interconnection of the mechanically stacked subcells is required for the two-terminal configuration as it is the case for the four-terminal configuration. Hence, installation costs of modules made from such cells are lower. If the costs can be reduced in the future, the presented results may therefore increase the market entrance chances for III-V/Si solar cells.

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