FRONT SIDE OPTIMIZATION ON BORON- AND GALLIUM-DOPED CZ-SI PERC SOLAR CELLS EXCEEDING 22% CONVERSION EFFICIENCY

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ABSTRACT: This work reviews on our industrial-oriented passivated emitter and rear cell (PERC) baseline process for Czochralski-grown silicon (Cz-Si) wafers at the Fraunhofer ISE PV-TEC pilot-line. We perform several front side optimizations based on homogeneous emitter doping: finger width reduction of the screen-printed silver fingers, improved silver paste, and implementation of low-temperature thermal oxidation. This yields peak energy conversion efficiencies of 22.1% for boron-doped Cz-Si from LONGi and 22.2% for gallium-doped Cz-Si from Fraunhofer CSP. We show that gallium-doped Cz-Si wafers offer an industrially feasible option to further improve PERC-type but also other solar cell concepts on p-type Cz-Si. We also demonstrate the possibility to omit regeneration procedures that are needed to suppress the boron-oxygen-related light-induced degradation effects as known for conventional boron-doped Cz-Si.
Keywords: PERC, front side optimization, screen printing, diffusion, Cz-Si, boron, gallium

1 INTRODUCTION

The passivated emitter and rear cell (PERC) [1] technology is the dominant technology in today's industrial solar cell mass production [2]. Thus, improving the energy conversion efficiency of PERC solar cells is of high interest to the photovoltaic community.

The aim of this work is to give a close-up insight into recent p-type silicon PERC technology that is being developed with industrial focus at Fraunhofer ISE's PV-TEC pilot-line [3,4]. Back in 2017, the optimization of the front side of PERC solar cells has been identified as the next step at Fraunhofer ISE to boost the efficiency to 22% and beyond [5]. After rebuilding the PV-TEC pilot-line that has been destroyed by a fire in early 2017 [3,6], we were able to proceed with front side optimizations.

In this work, we show improvements of the front side properties based on homogeneous emitter doping. We examine several optimization steps such as screen-printed finger width reduction on the front side, usage of a more up-to-date silver paste, incorporation of low-temperature thermal oxidation for improved emitter passivation, and the formation of an alternative emitter doping with lower surface charge carrier concentration. We also examine the usage of gallium-doped Czochralski-grown silicon (Cz-Si:Ga) wafers in comparison to conventionally boron-doped ones, i.e. Cz-Si:B.

2 PERC BASELINE FABRICATION PROCESS

2.1 PERC solar cells

The process sequence shown in Fig. 1 illustrates the PERC baseline process at the time when the experiment was carried out in the PV-TEC pilot-line at Fraunhofer ISE. In comparison to our PERC baseline process prior to the fire back in 2017 [5], we now use almost completely new tools (only two tools for passivation have already been used in 2017). Additionally, we switch from magnetically-cast Cz-Si:B in M0 wafer format to standard Cz-Si:B in M2 wafer format and we add an ultrafast regeneration process to the process sequence after contact firing. All tools until passivation are located in one laboratory, the PV-TEC Front End, and all tools from rear side local contact opening on are located at another laboratory, the PV-TEC Back End [3].

In this work, conventional p-type Cz-Si:B wafers with pseudo-square M2 wafer format (156.75 mm edge length, 210 mm diameter) and a base doping $\rho_b = 0.8\ \Omega$cm serve as starting material for the PERC fabrication. After alkaline texturing (consisting of saw-damage etching, texturing, and surface cleaning), a tube furnace diffusion using phosphorus oxychloride ($POCl_3$) as liquid dopant precursor forms the homogeneous emitter with an emitter sheet resistance $R_{sh} \approx 90\ \Omega$/sq. The $POCl_3$ diffusion is an industrial relevant process featuring an in-situ oxidation step. It is based on the diffusion process reported in Ref. [7] with minor process adjustments in a new tube furnace tool.

Subsequently, an inline wet-chemical etching process removes the rear emitter and the phosphosilicate glass (PSG)/silicon dioxide (SiO_2) layer stack. A wet-chemical cleaning step precedes surface passivation. The rear surface passivation layer consists of a 6 nm-thin aluminium oxide (Al_2O_3) layer deposited using a commercial, inline spatial atomic layer deposition (ALD) reactor [8], followed by an outgassing step in a tube furnace in nitrogen atmosphere at 550°C for 10 minutes. A 150 nm-thick silicon nitride (SiN_X) layer, deposited by plasma enhanced chemical vapor deposition (PECVD) [9], serves as capping layer on top of the Al_2O_3 layer. The front side is capped by a 75 nm-thick PECVD SiN_X layer serving as anti-reflection coating and surface passivation.

Figure 1: Schematic process sequence of the PERC baseline fabrication process at Fraunhofer ISE prior to the performed optimizations that are discussed within this work (ALD: atomic layer deposition, PECVD: plasma enhanced chemical vapor deposition).

An infrared laser process locally removes the rear layer stack in order to form dot-shaped local contact openings (LCO) in square arrangement parallel to the wafer edges with a pitch individually adapted to the base resistivity.

The rear and front metallization is applied using screen printing with commercially available metal pastes. In this work, no rear side silver pads are realized. The rear electrode is full-area printed using an aluminum-containing paste. The busbarless front silver grid features 110 fingers at a nominal screen opening of 33 µm. The average measured finger width after firing is $w_f \approx 38$ µm. Contact firing is performed in an industrial conveyor belt furnace with varying the peak temperature and the PERC cells are regenerated by an ultrafast inline regeneration process to mitigate boron-oxygen (BO) related light-induced degradation (LID) [10]. Finally, the current-voltage measurements are performed in an inline cell tester prior and after LID.

2.2 Test samples and characterization methods

Charge carrier concentration profiles after wet-chemical removal of the PSG/SiO_2 layer stack are obtained using the electrochemical capacitance-voltage (ECV) technique [11]. The surface roughness needs to be taken into account as the samples are alkaline textured. The measured charge carrier concentration profiles are corrected to match the emitter sheet resistance $R_{sh,4pp}$ (determined by four point probe (4pp) technique near the ECV spot) by applying the procedure described in Ref. [12].

The emitter dark saturation current density j_{0e} of the phosphorous emitter is examined on symmetrically alkaline textured n-type Cz-Si lifetime samples with a base resistivity $\rho_b = 6.5$ Ωcm. Although the j_{0e} samples do not feature an Al_2O_3 passivation layer, the outgassing step is performed to resemble the cell fabrication process; see Fig. 1. Then, the front and rear surfaces are passivated by the 75 nm-thick PECVD SiN_X layer and a firing step activates the passivation properties. Quasi-steady-state photoconductance (QSSPC) measurements are performed and evaluated with the procedure from Ref. [13].

The potential of the PERC precursors after passivation is examined by measuring the implied open-circuit voltage iV_{OC} by QSSPC. Therefore, the passivated PERC samples are fired without metallization in order to activate the passivation layer properties.

To determine specific contact resistances ρ_C, measurements according to the transfer length method (TLM) [14] are performed. The 1 cm-wide TLM strips are cut from completely processed PERC solar cells.

3 OPTIMIZATION APPROACH

Starting from our PERC baseline fabrication process as discussed in the previous chapter, we perform five optimization steps (1) - (5) to improve the front side properties. For all cells discussed in this work, we apply a homogeneously-doped front side emitter.

Fig. 2 shows the conducted optimizations and the respective cell groups Gr1 - Gr5:

(1) The screen-printed finger width is decreased by downsizing the nominal screen opening from 33 µm (360-16 mesh, Ref) to 24 µm (440-13 mesh, Gr1). This goes in hand with an increase in finger number from 110 to 120. Both screens feature busbarless metallization grids.

(2) We apply for Gr2 - Gr5 an improved version of a commercially available screen printing silver paste compared to the older version of the same supplier for Gr1.

(3) Low-temperature thermal oxidation is added as of Gr3 to obtain improved emitter passivation.

(4) The silicon base material is changed from boron-doped Cz-Si (Cz-Si:B) wafers with $\rho_b = 0.8$ Ωcm (produced by LONGi) to gallium-doped Cz-Si (Cz-Si:Ga) wafers with $\rho_b = 1.1$ Ωcm as of Gr4 (produced by Fraunhofer CSP). We decrease the x-y-pitch for the dot-shaped LCOs from $p_{LCO} = 500$ µm (Cz-Si:B) to $p_{LCO} = 425$ µm (Cz-Si:Ga). This doping-type change is also meant to suppress BO-related LID without the need to apply an additional regeneration process for Gr4.

(5) By adapting the $POCl_3$ diffusion in Gr5, we increase the emitter sheet resistance from $R_{sh} \approx 90$ Ω/sq to $R_{sh} \approx 110$ Ω/sq by decreasing the surface charge carrier density N_{surf}. This aims at decreasing the emitter dark saturation current density j_{0e} in the passivated emitter region.

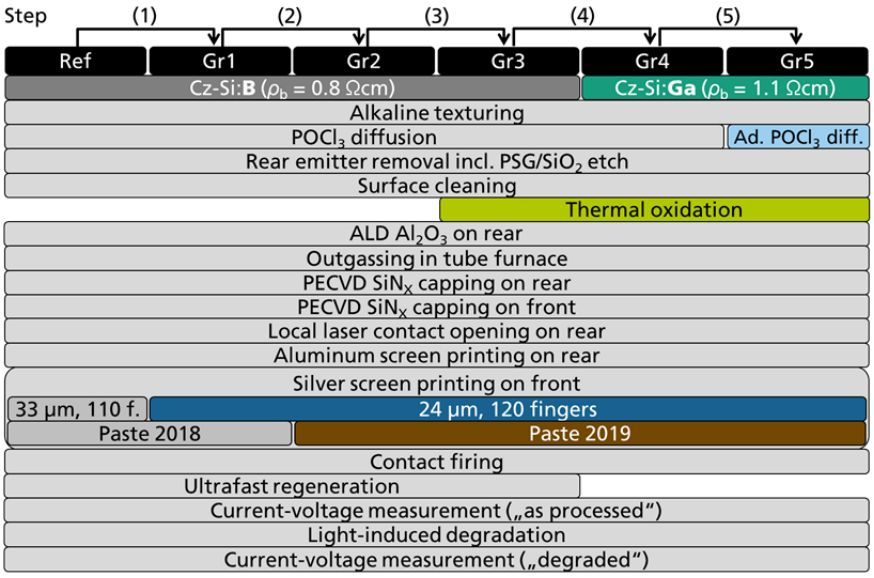

Figure 2: Schematic process sequences for the performed optimizations within this paper. The baseline PERC process from Fig. 1 is displayed far left in group Ref. The optimizations steps (1) - (5) are indicated on top of the group labelings.

4 RESULTS

4.1 Solar cell performance parameters resulting from illuminated current-voltage measurements

Fig. 3 shows the current-voltage data for the fabricated PERC solar cells from group Ref as well as Gr1 - Gr5 according to the process flow in Fig. 2. Only the data for the best performing firing temperature is considered, which is the same for all groups.

The performed optimization steps demonstrate an increase in energy conversion efficiency η by 0.4%$_{abs}$, starting from η = 21.8% for the reference group Ref and peaking at η = 22.2% for Gr4. For Gr5, however, the benefits of the adapted $POCl_3$ diffusion (lowest emitter dark saturation current density j_{0e} and highest implied open-circuit voltage iV_{OC} of all groups as will be discussed later) could not yet be transferred to improved solar cell efficiency levels. Detailed comparisons of the different optimization steps follow in the next section.

The current-voltage data of the champion PERC solar cells with an efficiency of 22.1% and 22.2% for Cz-Si:B and Cz-Si:Ga, respectively, are summarized in Table I.

Table I: Illuminated current-voltage parameters of the most efficient PERC solar cells from Gr3 and Gr4 measured with PCBtouch. Gr3 is measured by Fraunhofer ISE CalLab PV Cells. The inline cell tester measurement for the cell of Gr4 is calibrated based on the CalLab measurement of the cell from Gr3.

Gr.	Silicon type	η (%)	j_{SC} (mA/cm²)	V_{OC} (mV)	*FF* (%)	*pFF* (%)	r_S (Ωcm²)
3	Cz-Si:B	22.1	40.3	680	80.8	82.9	0.40
4	Cz-Si:Ga	22.2	40.4	679	81.1	83.1	0.39

4.2 Detailed results for the optimization steps

4.2.1 Step (1) - Smaller screen opening

By decreasing the nominal finger opening in the screen from 33 µm to 24 µm, the screen-printed and fired silver finger width after firing decreases from 38 µm to 32 µm. Fig. 4 shows the corresponding images of the screen-printed fingers for both screens after contact firing.

Despite an increase of the finger number from 110 fingers for group Ref to 120 fingers for group Gr1, the metallization fraction is decreased by about 8%$_{rel.}$, which leads to an increase in short-circuit current density j_{SC} of 0.15 mA/cm²; see Fig. 3. The fill factor *FF* and the open-circuit voltage V_{OC} remain constant. At the same time, the silver paste consumption reduces from 66 mg to 55 mg per cell. In total, the finger width reduction leads to an efficiency gain of 0.15%$_{abs}$.

4.2.2 Step (2) - Newer silver paste

The update of the front silver paste leads to somewhat smaller finger widths of 30 µm after contact firing for Gr2. Apart from a narrower *FF* distribution, no significant differences in the solar cell parameters are seen when comparing Gr2 (new silver paste) to Gr1 (old silver paste).

4.2.3 Step (3) - Thermal oxidation

The front-end processing is changed for Gr2 to Gr3 by incorporating a low-temperature thermal oxidation prior to the rear side Al_2O_3 deposition. As can be seen from Fig. 5,

Figure 4: Microscope images of the screen-printed fingers after contact firing for (left) group Ref with 33 µm screen opening and (right) group Gr1 with 24 µm screen opening.

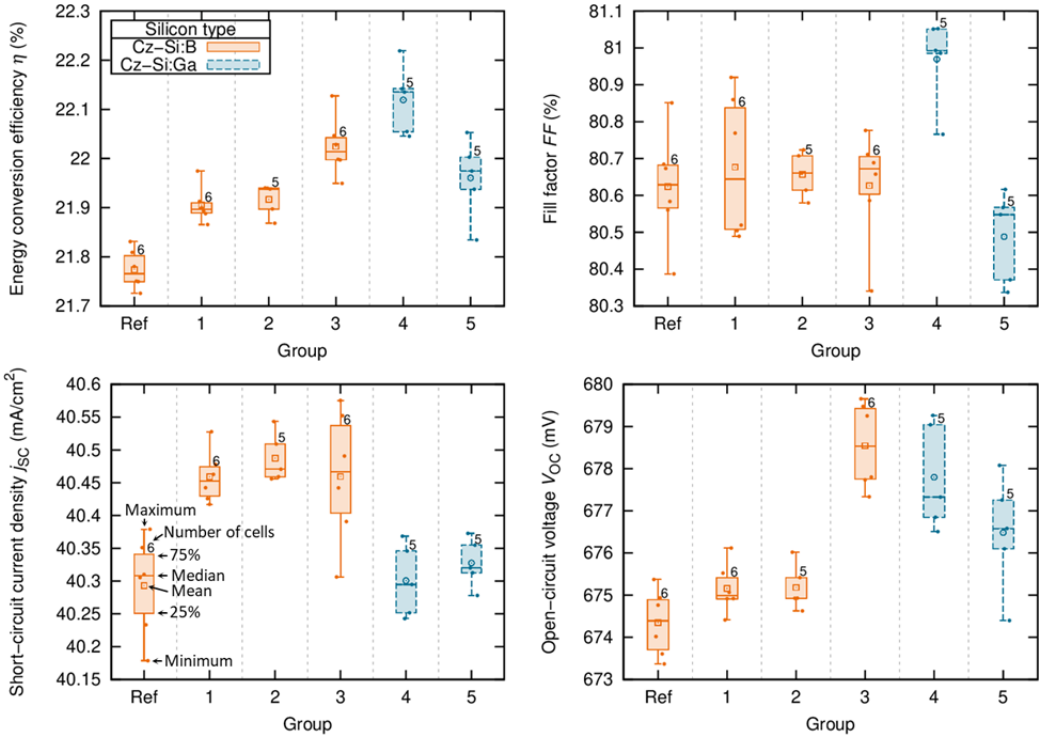

Figure 3: Parameters from AM1.5 illuminated current-voltage characterization of the PERC cells in the as processed state. The inline cell tester measurements are performed using PCBtouch contacting. The data is calibrated to a PERC cell measured at Fraunhofer ISE CalLab PV Cells. The meaning of the box plots is exemplary explained for the first data set at the bottom left.

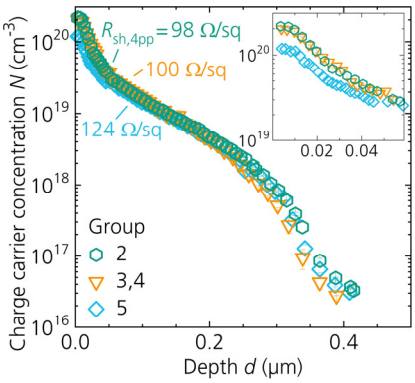

Figure 5: Emitter charge carrier concentration profiles measured by ECV on textured surfaces after PSG and SiO_2 removal. The data for group 2 also represents the groups Ref and Gr1. The inlay on the top right shows the magnification near the surface.

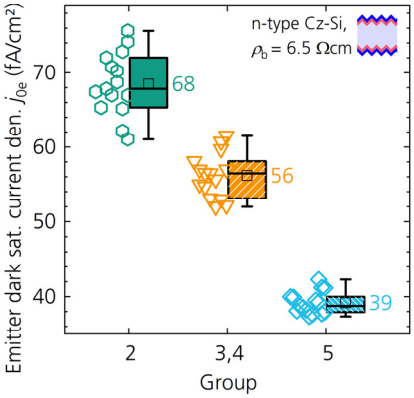

Figure 6: Emitter dark saturation current density j_{0e} for symmetrically alkaline textured and passivated n-type Cz-Si wafers after firing. The data for group 2 represents also the j_{0e} of groups Ref and Gr1. For each group, three samples are measured at five positions each. The numbers in the graph give the mean j_{0e} for each group.

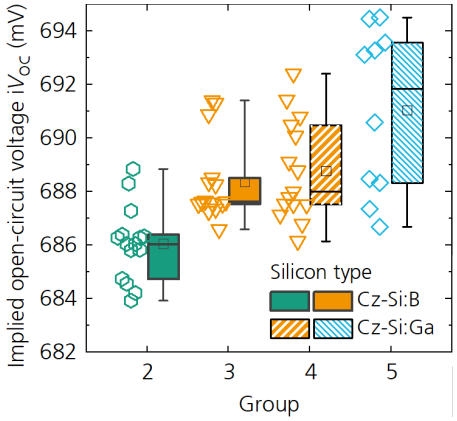

Figure 7: Implied open-circuit voltage iV_{OC} measured by QSSPC after firing of cell precursors without metallization. The data for group 2 represents also the iV_{OC} of groups Ref and Gr1. For each group, two to three samples are measured at five positions each.

this additional oxidation process has negligible impact on the emitter sheet resistance R_{sh} and the emitter charge carrier profile $N(d)$ with a surface charge carrier concentration $N_{surf} = 2{\cdot}10^{20}$ cm^{-3}. The grown SiO_2 layer yields an improved emitter passivation, which is expressed in a decrease in j_{0e} from $j_{0e} = (68 \pm 4)$ fA/cm² for Gr2 (without thermal oxidation) to $j_{0e} = (56 \pm 3)$ fA/cm² for Gr3 (with thermal oxidation); see also Fig. 6. The iV_{OC} also profits from thermal oxidation and increases in average by 2 mV to a mean iV_{OC} = 688 mV; see Fig. 7.

As shown in Fig. 3, the final PERC cells of Gr3 also benefit from the lower j_{0e} and higher iV_{OC} and the corresponding efficiency increase is 0.15%$_{abs}$ due to a significantly higher V_{OC} compared to Gr2.

4.2.4 Step (4) - Change of base material

We change the silicon base material to Cz-Si:Ga wafers that have been grown and sliced by Fraunhofer CSP. Fig 7 shows that the iV_{OC} for groups Gr3 (Cz-Si:B) and Gr4 (Cz-Si:Ga) are similar. Nevertheless, the current-voltage data in Fig. 3 yield an efficiency gain for the Cz-Si:Ga PERC solar cells (Gr4) of 0.1%$_{abs}$. The slightly lower j_{SC} for the Cz-Si:Ga cells (Gr4) is assigned to the fact that the Cz-Si:Ga wafers are 160 µm thick (measured prior to $POCl_3$ diffusion) and thus 4 µm thinner than the Cz Si:B wafers. The lower j_{SC} is overcompensated by a *FF* gain, which comes in equal parts from increased *pFF* as well as from decreased series resistance r_S (not shown).

Concerning BO-related LID, we reduce the efficiency drop for the Cz-Si:B cells (Ref, Gr1 - Gr3) to only 0.1%$_{abs}$ (not shown) by performing the ultrafast regeneration process after contact firing. However, for the Cz-Si:Ga cells (Gr4) for which no regeneration process has been performed, no LID is observed at all. Hence, using Cz-Si:Ga material makes the regeneration process obsolete.

4.2.5 Step (5) - Adapted $POCl_3$ diffusion

The adapted $POCl_3$ diffusion of Gr5 yields an emitter charge carrier profile that is only changed near the silicon surface compared to the profiles from Ref and Gr1 - Gr4. As is seen from the ECV profiles in Fig. 5, the profile depth is not changed. The inlay in Fig. 5 illustrates that N_{surf} is decreased to $N_{surf} = 1{\cdot}10^{20}$ cm^{-3} leading to an increase in R_{sh} of about 20 Ω/sq compared to Gr3,4 (standard $POCl_3$ diffusion).

The lower N_{surf} allows for less charge carrier recombination in the emitter. The j_{0e} decreases significantly to $j_{0e} = (39 \pm 2)$ fA/cm² for Gr5 (adapted $POCl_3$ diffusion with thermal oxidation); see Fig. 6. The iV_{OC} increases by 3 mV to a mean iV_{OC} = 691 mV and peak iV_{OC} = 695 mV; see Fig. 7.

However, these improved properties of the PERC precursors of Gr5 do not lead to a higher efficiency of the finalized cell devices. On the contrary, mainly due to a 0.5%$_{abs}$ lower *FF*, the efficiency drops by 0.15%$_{abs}$ from Gr4 (standard $POCl_3$ diffusion) to Gr5 (adapted $POCl_3$ diffusion). This *FF* loss results from a 0.2%$_{abs}$ lower pseudo fill factor *pFF*. The remaining 0.3%$_{abs}$ *FF* loss originates from a higher series resistance r_S: r_S(Gr4) = 0.41 Ωcm² and r_S(Gr5) = 0.48 Ωcm².

Fig. 8 elucidates that the decrease in N_{surf} for Gr5 leads to a somewhat larger contact resistivity ρ_C. Although $\rho_C = (1.3 \pm 0.8)$ mΩcm² for Gr5 is twice as high as $\rho_C = (0.6 \pm 0.3)$ mΩcm² for Gr4, it is still very low. The larger ρ_C and the larger R_{sh} for Gr5 each contribute half to the r_S-related lower *FF* of 0.3%$_{abs}$.

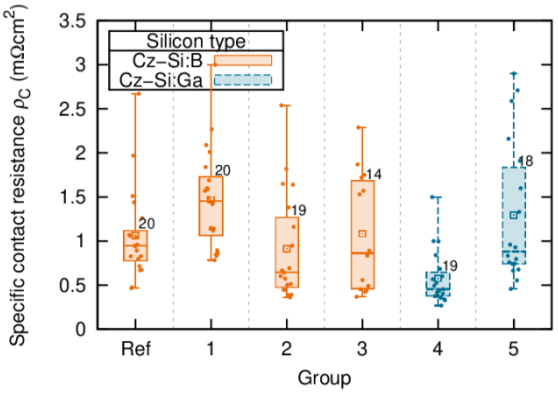

Figure 8: Specific contact resistances ρ_C measured by TLM on finished PERC solar cells from the different groups. The numbers in the graph indicate the number of TLM measurements for each group.

On the other hand, also the V_{OC} is lower despite higher iV_{OC}. This suggests that the dark saturation current density in the metallized areas $j_{0,met}$ is increased due to the lower N_{surf} and, hence, results in weaker shielding of charge carriers from the recombination-active surface. This is confirmed by numerical simulations using a freeware tool [15] assuming a surface recombination velocity of 10^7 cm/s giving emitter dark saturation current densities $j_{0,met} \approx 500$ fA/cm² for the standard diffusion without thermal oxidation (Ref, Gr1,2) and with thermal oxidation (Gr3,4), and of $j_{0,met} \approx 900$ fA/cm² for the adapted diffusion with thermal oxidation (Gr5).

5 SUMMARY AND CONCLUSION

Our industrial-oriented PERC baseline shows stable and reproducible results by which we process Cz-Si PERC solar cells in M2 wafer format and busbarless metallization.

By stepwise optimizing the front side properties and the used bulk material in five steps, we demonstrate an energy efficiency increase of 0.4%$_{abs}$ resulting in 22.2% efficient Cz-Si:Ga PERC solar cells with homogeneous emitter.

We decrease the screen-printed silver finger width on the front side after firing from 38 µm to 32 µm which reduces the silver paste consumption from 66 mg to 55 mg per cell.

Incorporating a low-temperature thermal oxidation prior to rear side aluminum oxide deposition yields an improved emitter passivation due to the grown silicon dioxide layer. The emitter dark saturation current density on our standard $POCl_3$ emitter decreases from $j_{0e} = (68 \pm 4)$ fA/cm² without oxidation to $j_{0e} = (56 \pm 3)$ fA/cm² with oxidation at a surface doping concentration of about $2 \cdot 10^{20}$ cm^{-3}. Thereby, the performed low-temperature oxidation has negligible impact on the emitter sheet resistance and the emitter doping profile.

The PERC cells on Cz-Si:Ga wafers produced by Fraunhofer CSP show a 0.1%$_{abs}$ higher efficiency in comparison to the Cz-Si:B PERC devices with LONGi material peaking at 22.1% efficiency. By applying an inline ultrafast regeneration process, we reduce the efficiency drop for the Cz-Si:B devices due to boron-oxygen-related light-induced degradation (LID) to only 0.1%$_{abs}$. Without a regeneration process, no LID at all is observed for the Cz-Si:Ga PERC cells. Hence, this process step is not needed for Cz-Si:Ga PERC cells.

On the basis of the presented results, we could significantly improve our PERC baseline process which now features thermal oxide emitter passivation and narrower contact fingers on the front side.

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