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HYDROSILANE-FREE LOW-COST APCVD OF SIO_2 FILMS FOR CRYSTALLINE SI SOLAR CELL APPLICATIONS

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ABSTRACT: A SiH_4-free atmospheric pressure chemical vapor deposition (APCVD) technique was developed that provides a simple, flexible and cost-effective approach for the preparation of SiO_2 coatings at room temperature. Microscopic investigations revealed that the deposited films are smooth and dense. No pinholes in the SiO_2 coatings or gaps between the SiO_2 and the substrate were found. On 6 inch Si wafers, the obtained SiO_2 thickness variation was ± 10 %. After densification at 400 °C for a few minutes the layers are well suited for protective coatings in various applications. We successfully demonstrated i) single-side texturing of monocrystalline Si wafers and ii) elimination of parasitic metal deposition during electroplating of crystalline Si solar cells' front side metallization.

Keywords: SiO_2, Atmospheric Pressure Chemical Vapor Deposition, Protective Coating

1 INTRODUCTION

There are several well-known techniques for the deposition of SiO_2 films like low-pressure chemical vapour deposition (LPCVD), plasma-enhanced chemical vapour deposition (PECVD), atomic layer deposition (ALD), spray pyrolysis (SP), sol-gel deposition (SGD) and atmospheric pressure chemical vapour deposition (APCVD). Probably the most widespread technique is PECVD. However, at low substrate temperature the SiO_2 films prepared this way tend to be porous [1]. They can be employed as optical coatings on glass because of their low refractive index, but often dense SiO_2 films and hence high deposition temperatures are desired, e. g. if protective coatings are needed. Apart from the high deposition temperature another cost driver for the equipment price is the vacuum system. SP, SGD and APCVD operate at atmospheric pressure and hence are favourable when it comes to costs. Among those APCVD has the advantage of using gases as precursors in contrast to liquids. Hence, crack-free dense films with good step coverage can readily be obtained. Common APCVD of SiO_2 utilizes the reactants hydrosilane (SiH_4) and dinitrogenmonoxide (N_2O) at deposition temperatures between 250 °C and 400 °C [2]. Because SiH_4 immediately catches fire when it comes into contact with air special precautions are required. In our newly developed setup we utilize a SiH_4-free SiO_2 APCVD technique that operates at room temperature. By subsequent annealing of the films at temperatures up to 400 °C for a few minutes their etch rate is minimized, making them well suited for protective coatings in various applications. In this work we demonstrate single-side alkaline texturing of monocrystalline Si wafers and reduction of parasitic metal deposition during electroplating of crystalline Si solar cells' front side metallization.

2 EXPERIMENTAL

The low process temperature allows for manufacturing the deposition equipment completely from plastic. This has the additional advantage of easy elimination of possible metal contamination. We utilized fused deposition modeling so that the device can flexibly be adapted to e. g. different wafer sizes. The thermoplastic material used in the 3D printing process was polylactic acid. Our present setup is a single wafer reactor suitable for 6 inch wafers. The reactive gases are mixed in a chamber and form SiO_2 films on the substrate, see Figure 1. The ratio of the SiO_2 layer thickness on the front side to that on the back side can be adjusted by varying the distance between the wafer and the base plate of the deposition chamber. In the applications investigated in this work the wafers and cells were positioned directly on the base plate (label 4 in Fig. 1) in order to ensure single-side SiO_2 coating. In a possible inline deposition system, the cells could be placed on a gas-tight conveyor belt.

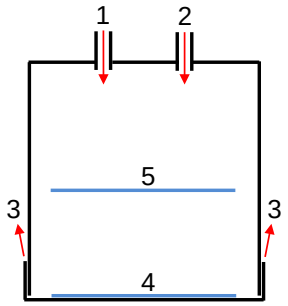

Fig. 1: Schematic cross-section drawing of the lab-type SiO_2 APCVD setup. 1) Inlet of gas 1, 2) inlet of gas 2, 3) exhaust, 4) wafer position for deposition on the upper wafer side only, 5) wafer position for simultaneous deposition on upper and lower wafer side.

The deposition rate is set by changing the gas flow rates. Values from 15 to 245 nm/min were obtained. The gas consumption per SiO_2 thickness depends on the gas composition. Using optimized parameters for our laboratory setup, the cost of gases was approximately 1 \$Cent per 100 nm thick SiO_2 layer on a 245.7 cm² Si wafer.

In our first application, one-sided alkaline texturing, we coated shiny etched 6 inch CZ Si wafers on one side with about 120 nm SiO_2 in 1 min at room temperature. The wafers were then annealed for 1 min on a hotplate at 400 °C to densify the SiO_2. Finally, the wafers were immersed in an aqueous texturing solution containing 1.5 wt% NaOH and a texture additive for 6 min at 80 °C.

Our second application is the elimination of parasitic plating during electrochemical deposition of the front side metallization on Si solar cells. We used alkaline textured *p*-type passivated emitter and rear contacted (PERC) CZ Si solar cells with screen-printed full-area Al backside metallization and Si_xN_y antireflection coating (ARC) on the front. SiO_2 with a thickness of about 90 nm was deposited on the Si_xN_y ARC and annealed at 400 °C for 10 min. In order to clearly recognize the effect of the SiO_2, it was deposited locally with a shadow mask. On the front side, a 5 busbars and 110 fingers contact grid layout was laser ablated, the cells were immersed in 1.5 wt% HF for 20 s and galvanized with a Ni/Cu/Ag metal stack.

The uniformity of the thickness of the deposited SiO_2 layers was measured on shiny etched wafers by ellipsometry. Furthermore, the microstructure of the layers was examined in a secondary electron microscope (SEM) and the performance of the alkaline texture was characterised by hemispherical reflectance measurements using an integrating sphere.

3 RESULTS AND DISCUSSION

3.1 SiO_2 thickness uniformity, refractive index and microstructure

Fig. 2 shows photos of both sides of a shiny-etched 6 inch CZ Si wafer after APCVD of SiO_2. The wafer was placed on the base plate of the APCVD device during deposition to minimize the SiO_2 layer thickness on the backside. This position has the label 4 in Fig. 1. The numbers in Fig. 2 indicate the thickness of the SiO_2 layer, measured by ellipsometry at the respective position on the photos. The thickness uniformity obtained is 89 ± 7 nm on the front side, corresponding to a relative variation of ± 8 %. The SiO_2 thickness on the rear side reaches a maximum value of 5 nm at one edge of the wafer. At this point, the wafer stood slightly away from the base plate of the device.

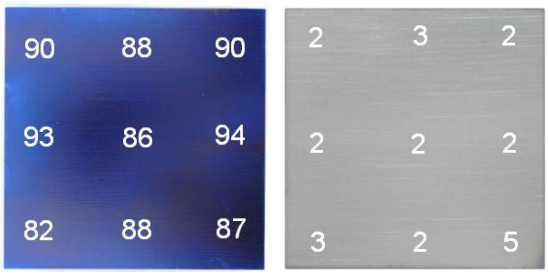

Fig. 2: Photos of a smooth 6 inch CZ Si wafer after APCVD of SiO_2 at room temperature showing the film thickness in nm measured by ellipsometry. **Left:** Upper wafer side. **Right:** Lower wafer side that was positioned on the base plate of the deposition chamber. Note that the horizontal lines visible in the photos are reflections of saw marks on the wafers and are not correlated with the APCVD process.

Fig. 3 depicts photos of a shiny-etched CZ Si wafer which was in the upper position with the label 5 in Fig. 1 during SiO_2 deposition. The distance between wafer and base plate was 55 mm. The wafer was only held locally at the edge in order to obtain a uniform SiO_2 layer on the lower side as well. The measured SiO_2 thickness variation is 86 ± 9 nm on the upper and 54 ± 3 nm on the lower wafer side, which corresponds to relative values of ± 10 % and ± 6 %, respectively. The two-sided deposition mode can be used, for example, when insulating plating masks are required on both sides of the wafer.

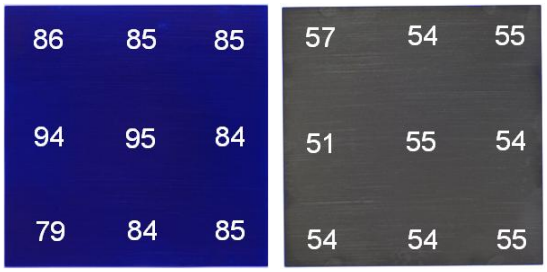

Fig. 3: Photos and SiO_2 thickness map of the upper side (left) and lower side (right) of a smooth 6 inch CZ Si wafer. The wafer was placed during APCVD of SiO_2 at a distance of 55 mm from the bottom plate.

A comparison between the refractive index of as deposited APCVD SiO_2 and that of thermal SiO_2, measured by ellipsometry in the wavelength range from 300 to 1000 nm, is shown in Fig. 4. It can be seen from the figure, that the refractive index of APCVD SiO_2 in the entire wavelength range is 0.02 lower than that of thermal SiO_2. This can be explained by the assumption of a slightly lower density of the APCVD SiO_2 layer.

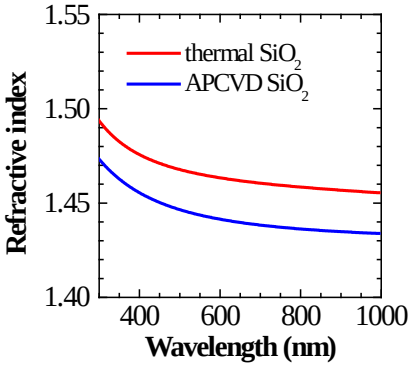

Fig. 4: Measured refractive index of APCVD SiO_2 and thermal SiO_2 as a function of wavelength.

In order to investigate the microstructure of the APCVD SiO_2 films, very thick layers were deposited on polished FZ Si. Cross sections were prepared by ion milling and examined in a SEM. The obtained images are depicted in Fig. 5. Both the 575 nm and the 764 nm thick SiO_2 film are dense and smooth. No cavities were found in the films and no gaps between SiO_2 coating and Si substrate.

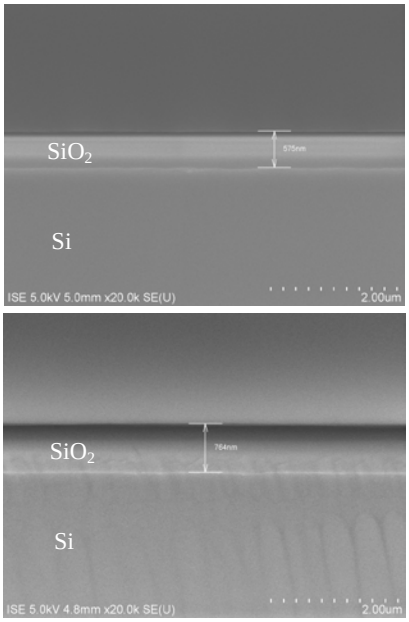

Fig. 5: SEM images taken of cross sections of thick APCVD SiO_2 films deposited on polished FZ Si wafers.

3.2 APCVD SiO_2 as etching barrier

The thickness uniformity demonstrated above allows us to apply the SiO_2 layers on 6 inch wafers without restrictions. In preliminary tests, we found that SiO_2 layers densified at 400 °C for 1 min withstand the alkaline texturing solution for more than 6 min if the SiO_2 films are thicker than about 80 nm. To ensure good process reliability, we regularly apply 120 nm thick layers in 1 min. Photos of both sides of a 6 inch CZ Si wafer after texturing and subsequent etching the SiO_2 layer in 20 wt% HF in 30 s are shown in Fig. 6. It can be seen that a uniform surface texture was formed on the uncoated front side. A thin SiO_2 layer like the one shown in Fig. 2 on the right, which is unintentionally deposited on the underside of the wafer, has no negative effect on texturing as it is easy to etch off. The other side of the wafer, which was protected by a 120 nm thick SiO_2 layer, is smooth as intended. By inspection with an optical microscope we did not find any local texture there. Hence, we conclude that the SiO_2 films can be deposited on large area without pinholes.

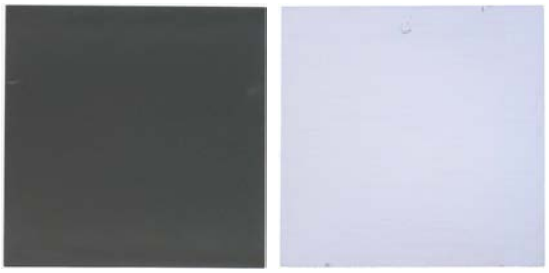

Fig. 6: Photos of the front (left) and the rear sides (right) of a 6 inch CZ Si wafer after alkaline texturing. The rear side was protected by an APCVD SiO_2 layer, which was subsequently etched in HF.

Fig. 7 shows SEM images of both sides of a FZ Si wafer after the one-sided texturing process as described before. In accordance with the above results we found uniformly distributed random pyramids on the textured side and no traces of etching attack on the other side.

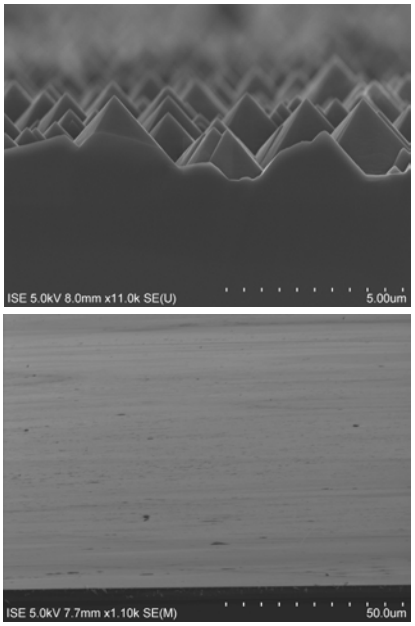

Fig. 7: SEM images of the front (top) and rear (bottom) of a one-side textured FZ Si wafer using an APCVD SiO_2 etching barrier.

Because the optical properties are rather sensitive to the surface morphology we measured the hemispherical reflectance of the textured and the smooth surface of the FZ Si wafer shown in Fig. 7. The obtained curves are plotted in Fig. 8. Please note that the SiO_2 layer is still on the smooth back, i. e. it was not etched by HF after alkaline texturing.

The measured reflectance of the textured surface is compared to the one of a reference wafer that was texture etched without SiO_2 coating on the rear. The figure shows that the curves are almost identical. When it comes to the smooth surface of the one-sided textured wafer we compare the measured reflectance with the one calculated by the transfer-matrix algorithm [3] assuming 84 nm thick thermal oxide grown on flat crystalline Si. The curves are the same within the measurement error. Again we can conclude that the APCVD SiO_2 layer was deposited without pinholes and is a stable etching barrier against the alkaline texturing solution.

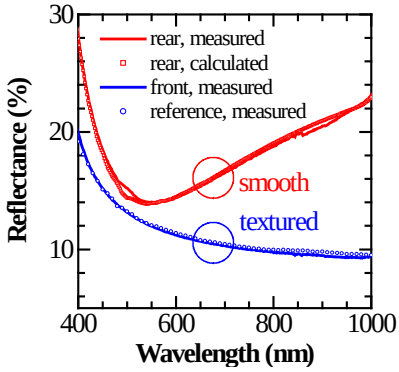

Fig. 8: Hemispherical reflectance measured on both sides of the one-sided textured FZ Si wafer depicted in Fig. 7 in comparison to reference values. Note that there was an approximately 84 nm thick SiO_2 layer on the smooth rear side.

3.3 APCVD SiO_2 as electrically insulating layer

Ni/Cu/Ag plating of the front side grid on c-Si solar cells significantly reduces the Ag consumption compared to screen-printing and provides very low contact resistance to low-doped emitters. Due to the potential cost reduction and efficiency increase plating is very attractive for solar cell production. Sometimes, however, the Si_xN_y antireflection coating on the cells is not well suited as a plating mask. The reasons for this are i) pinholes in the Si_xN_y which are formed from particles that detach from the deposition chamber and fall onto the cells, ii) microscopically small blisters in the Si_xN_y which can occur during sintering of the screen-printed rear contact or iii) scratches due to handling. In these cases, parasitic plating takes place outside the laser-ablated contact grid, so that the yield in solar cell production decreases.

In order to offer a cost-effective technical solution, we applied 90 nm thick SiO_2 on top of the Si_xN_y ARC by APCVD and densified the layer for 10 min at 400 °C right before laser ablation of the contact grid layout. Fig 9 is a photo of a part of a solar cell after Ni/Cu/Ag plating on which the SiO_2 had been deposited locally. It is clearly visible that the area with the Si_xN_y antireflection coating only reveals massive parasitic plating in between the finger lines. In contrast, the additional SiO_2 coated area of the cell has virtually no parasitic plating.

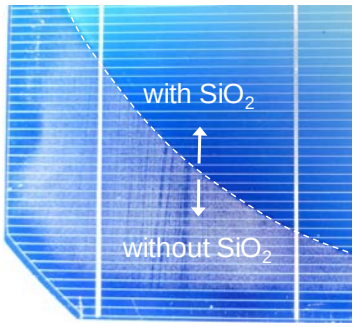

Fig. 9: Photo of a part of an alkaline textured CZ PERC Si solar cell after plating of the front side metallization.

It is interesting to note that in the illuminated *IV* measurement the APCVD SiO_2 acts as a second antireflection coating. Hence, the short circuit current density increases. After module integration with ethylene vinyl acetate or polyolefin encapsulation material, however, this optical effect is eliminated because the refractive indices of the encapsulation materials are similar to that of SiO_2.

4 SUMMARY AND CONCLUSION

SiH_4-free APCVD of SiO_2 at room temperature provides dense, smooth and uniform conformal coatings without pinholes on large surfaces. High deposition rates of up to 245 nm/min have been achieved. After densification at a temperature of 400 °C for up to 10 min, the coatings act as an efficient etching barrier against alkaline texturing solution and as insulating layer against parasitic plating in the electrochemical metallization process of c-Si solar cells. The successful application as plating mask on transparent conducting oxide coated Si heterojunction solar cells is demonstrated in [4].

Since the developed APCVD system operates at room temperature and can be made from plastic, the investment costs are low. In addition, the operating costs a relatively low when you consider that the cost of gases is about 1 $Cent per 100 nm thick SiO_2 layer on a 245.7 cm² large Si wafer in the laboratory system.

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5 REFERENCES

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