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CONTACT RESISTIVITY OF THE TCO/A-SI:H/C-SI HETEROJUNCTION

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ABSTRACT: Transport related losses in the heterojunction stack are a limitation on the power output of silicon heterojunction solar cells. We present contact resistivity measurements of the electron and hole contact of our silicon heterojunctions, which enable fill factors above 80 % on cell level. Our systematic investigation of the influence of different layers reveals, that the intrinsic a-Si:H and the ITO layer significantly increases transport losses, especially for the hole contact. Experimental results are supported by good correlation with numerical device simulation.
Keywords: Silicon Heterojunction, Amorphous silicon, Contact resistivity

1 INTRODUCTION

The outstanding open-circuit voltage V_{oc} values of silicon heterojunction (SHJ) solar cells are owed to excellent passivation of the crystalline silicon (c-Si) surface by a thin hydrogenated amorphous silicon (a-Si:H) layer [1]. Limitations on cell performance arise from rather low short-circuit current density J_{sc} due to parasitic absorption in the amorphous silicon films at the front [2] and significant resistive losses (quantified by p*FF*-*FF* or the contact resistivity ρ_c) in the stack of TCO/a-Si:H(n/p)/a-Si:H(i) [3]. Better understanding regarding the cause of these transport losses is mandatory for a holistic device optimization.

In this work, we use easily fabricated contact resistance test structures to quantify vertical resistive losses in the heterojunction stack. Our dedicated resistance test structures enable us to investigate the influence of different layers. Experimental findings are supported by numerical device simulations described in [4]. For our in-depth investigation of transport losses at the TCO/a-Si:H/c-Si heterojunction including thermal stability and temperature dependent *I-V* measurements we refer to [5].

2 EXPERIMENTAL

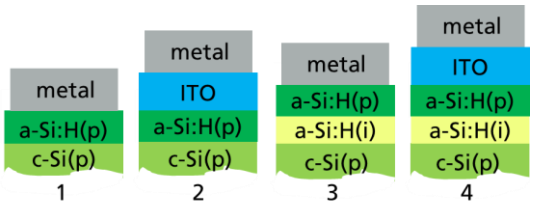

Figure 1: Sketch of the different resistance test structures used for the hole contact. For the electron contact, phosphor doped a-Si:H and c-Si bulk was used. The rear contact of all groups comprised the front side stack of group 1 and full area metallization.

200 (250) µm thick random pyramid textured 1 Ω·cm *n*-type (*p*-type) FZ silicon wafers were used as a substrate. After cleaning, doped and intrinsic a-Si:H layers were deposited via plasma-enhanced chemical vapor deposition (PECVD). On the rear side, a doped a-Si:H layer capped with a full-area stack of electron-beam evaporated TiPdAg served as low-ohmic rear contact. At the front side, 2.0x2.0 cm² TiPdAg windows were aligned with 2.2x2.2 cm² windows of sputtered ITO (groups 2 and 4 in Fig. 1) or directly evaporated on a-Si:H (groups 1 and 3) using shadow masks. Prior to the I-V measurements, the structures were annealed on a Präzitherm hotplate in ambient air at 180 °C for 10 min. Two-terminal *I-V* measurements were performed on a WAVELABS Sinus-220 at 25 °C.

3 RESULTS

For both hole and electron contact four test structures comprising different heterojunction stacks at the front were utilized (Fig. 1):

(1) Symmetrical samples with only doped a-Si:H(p/n) and metal at the front (and rear)
(2) Structure 1 with additional ITO layer between doped a-Si:H and metal
(3) Structure 1 with additional intrinsic a-Si:H layer between doped a-Si:H and c-Si bulk
(4) Device relevant stack including all intrinsic a-Si:H, doped a-Si:H and ITO layer

Between groups 1 and 2 the influence of the ITO and between groups 1 and 3 the influence of the a-Si:H(i) layer could be seen for the electron and hole contact.

The total resistance values R_t after 180 °C annealing including the c-Si bulk, the front and rear contact and the contact to the metal on both sides, were extracted from the slope of the dark *J-V* curve around zero voltage. Contributions from the c-Si bulk were subtracted according to nominal resistivity and thickness. Additionally, contributions from the rear side, which comprised the front side stack of group 1 for all groups, were also subtracted using the symmetrical group 1 structure as a reference. The influence from the metal/a-Si:H or metal/ITO contact was assumed to be negligible in this study.

In Fig. 2 the experimentally determined contact resistivity ρ_c of the front side stack is depicted for all groups and both polarities via box plots. Grey stars represent simulated resistance results of corresponding structures (data from [4]). Both group 1 reference structures nNn and pPp showed ohmic behaviour with low ρ_c values of ~0.1-7 mΩ·cm² for the electron contact and ~1-16 mΩ·cm² for the hole contact. For a solar cell with high V_{oc} and p*FF*, an intrinsic a-Si:H layer is

necessary for passivation of the c-Si surface. Including the a-Si:H(i) in our test structure (group 2) lead to an significant increase in ρ_c (~ +150 mΩ·cm²) for the hole contact. For the electron contact, the increase in ρ_c with additional intrinsic a-Si:H was much less pronounced (~ +10 mΩ·cm²).

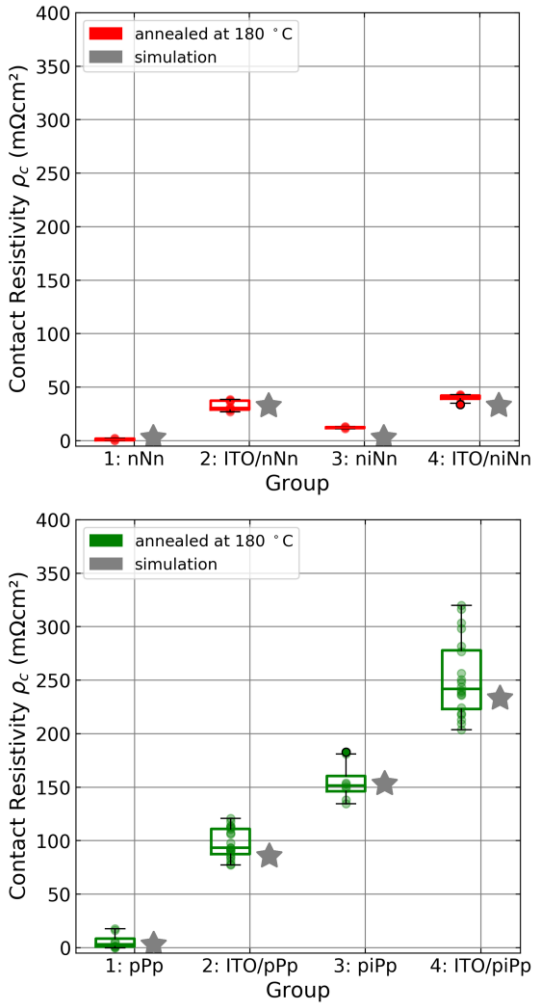

Figure 2: Contact resistivity ρ_c of different electron (red) and hole contact (green) heterojunction stacks after 180 °C annealing. Grey stars represent simulated data from [4].

Furthermore, for lateral transport and as anti-reflective coating a transparent conductive oxide (TCO, here ITO) is needed for a properly working device [2]. However, these beneficial properties come at the cost of higher vertical transport losses for both electron and hole contact. The hole contact resistivity $\rho_{c,p}$ increased by ~ 80 mΩ·cm² and the electron contact resistivity $\rho_{c,n}$ by ~ 30 mΩ·cm² with the addition of ITO (group 3). The increase in resistance with additional layers (both ITO and intrinsic a-Si:H) was accompanied with a transition from a linear (ohmic) to a non-linear (non-ohmic) *I-V*-characteristic (not shown here). For the device relevant stack (group 4) this resulted in minimum ρ_c values of 34 mΩ·cm² for the electron contact and ρ_c = 204 mΩ·cm² for the hole contact respectively. The finding of an significantly (six times) higher ρ_c of the hole contact compared to the electron contact is in line with results from several other groups investigating SHJ contacts (e.g. [3, 6, 7]).

A good agreement of experimental and simulated data was achieved (Fig. 2). The simulation reproduced the same trends obtained experimentally and absolute values coincided within experimental errors for all groups, except group 3 and 4 of the electron contact. It is worth noting, that the simulation yielded essentially the same resistance for group 1 and 3 of the electron contact i.e. whether or not the intrinsic a-Si:H layer is included.

4 DISCUSSION

It was observed, that the increase in ρ_c due to intrinsic a-Si:H is much more pronounced for the hole contact. One reason should be the higher (about three times [8]) valence band offset between a-Si:H and c-Si compared to the conduction band offset [9]. Therefore the transport barrier is higher for holes and tunneling is required, whereas the smaller barrier for electrons might be sufficiently low to be overcome by thermal emission. The low-ohmic nature of group 1 of the hole contact shows, that tunneling of holes across the junction between the highly-defective [10, 11] doped a-Si:H and the c-Si bulk is efficient. However, the higher screening-length in less-defective a-Si:H(i) lowers the tunnel probability and might be responsible for the strong increase in ρ_c for groups 3 and 4 of the hole contact.

The reason for a higher increase in ρ_c due to ITO (group 1 vs. group 2) for the hole contact compared to the electron contact is twofold. First, the work function difference between ITO and doped a-Si:H leads to a depleted interface, mainly on the a-Si:H side of the junction [12-15], since the charge carrier concentration is several orders of magnitude lower compared to the ITO. Sufficient doping and defects are necessary for a low depletion width i.e. effective tunneling [15, 16] and more easily achieved for phosphor doped a-Si:H due to the higher doping efficiency compared to boron doped a-Si:H [17]. Second, the ITO/a-Si:H(p) junction is unisotype, meaning that holes are the majority charge carriers on one side (a-Si:H(p)) and electrons on the other side of the junction (ITO). This makes the ITO/a-Si:H(p) interface a recombination junction, where holes in the a-Si:H(p) valence band have to recombine with electrons in the ITO conduction band [18, 19]. For that reason, trap states at suitable energy levels will play a vital role for efficient tunneling [20, 21]. A more detailed discussion about transport properties of the heterojunction stack for both electron and hole contact can be found in [5].

5 CONCLUSION

The influence of different layers on the contact resistivity ρ_c of the electron and hole contact of silicon heterojunctions was thoroughly studied on dedicated resistance test structures. Both, the intrinsic a-Si:H and the ITO layer increased ρ_c considerably, especially for the hole contact. This lead to a six times higher ρ_c for the device relevant hole contact stack compared to the electron contact. Experimental results were supplemented with numerical device simulations and possible implications on transport characteristics were discussed.

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