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OPTIMIZATION OF INLINE PROCESSES FOR THE PRODUCTION OF FREESTANDING EPITAXIALLY GROWN THIN FILMS FOR SOLAR CELLS

Alexey Ivanov, Ralf Sorgenfrei, Elke Gust, Philipp Barth, Kris Van Nieuwenhuysen*, Saskia Kühnhold-Pospischil, Stephan Riepe, Stefan Janz
Fraunhofer Institute for Solar Energy Systems (ISE), Heidenhofstrasse 2, D-79110 Freiburg, Germany
*imec v.z.w., Kapeldreef 75, B-3001 Leuven, Belgium

ABSTRACT: In this publication we discuss inline aspects of fabricating freestanding epitaxially grown thin silicon for solar cells. Especially the inline electrochemical porosification and its limitations are discussed and homogeneity improvements achieved with aid of electric simulations are presented. Different types of inhomogeneity for porous silicon layers lead to difficulties when forming a proper separation layer through reorganization and the detachment yield of the epitaxial thin film is affected. One of the solutions to ensure good detachment of the films is to form several local separation layers in a kind of puff pastry like structure where detachment of epitaxial film might proceed in any of the separation layers thus increasing yield. However, in case of too high porosity of the highly porous layer, large cavities without smaller supporting silicon pillars can collapse during reorganization and the surface layer can re-attach to the substrate making detachment of this area impossible. Additionally, local warping of the reorganized template before epitaxy can lead to detrimental defects like stacking faults.

KEYWORDS: Thin Film Solar Cell, Manufacturing and Processing, Porous Silicon, Epitaxy, electrochemical etching.

1 INTRODUCTION

The use of single crystalline flexible silicon thin films and foils is widespread throughout many applications like flexible IC chips [1], SOI [2] and solar cells [3] [4]. One of the technologies for those applications is the epitaxial growth on reorganized porous silicon substrates, which allows the subsequent detachment of the grown epilayer and reuse of the parent substrate. Especially for solar cells, this approach has been adopted to obtain large area epitaxial thin films in order to reduce material costs substantially while maintaining the efficiency potential of conventional mono wafers. A very important issue to lower the production costs is the consequent inline implementation of all single processes. At Fraunhofer ISE, the required core processes, inline porosification and inline epitaxy, have been developed and optimized in the last years.

In contrast to thick epitaxial wafers, the growth of detachable thin layers (EpiFoils) with thickness below 100 µm is more difficult due to handling issues and stronger influence from impurities of the substrate. We report the complete value chain from porosification, reorganization and epitaxy to characterization and detachment. The focus is to point out some limitations for production of high quality EpiFoils with high detachment yield. Finally, we present useful approaches to overcome the limitations.

2 EXPERIMENTAL AND CHARACTERIZATION METHODS

2.1 Fabrication steps

For the experiments, (100) silicon (Si) as-cut wafers of p-type with size 156×156 mm^2, thickness 550 µm, and resistivity of 10–15 mΩcm were used. Before porosification, standard damage etch (SDE) was performed. Alternatively in some cases chemical polishing was used to reduce surface roughness.

To form porous silicon (PorSi) layer, wafers were anodically etched in an experimental inline lab tool, capable to etch wafers up to 180 mm width and at least 156 mm length. The tool has been developed at Fraunhofer ISE in cooperation with RENA Technologies GmbH (Gütenbach, Germany). The schematic of the inline porosification tool is shown in Figure 1a. The setup consists of at least three electrolyte tanks, whereas the two side tanks are connected anodic and the middle one connected cathodic. As electrodes, glossy carbon cylindrical electrodes are used. The tanks of opposite polarity are isolated from each other by an air gap /

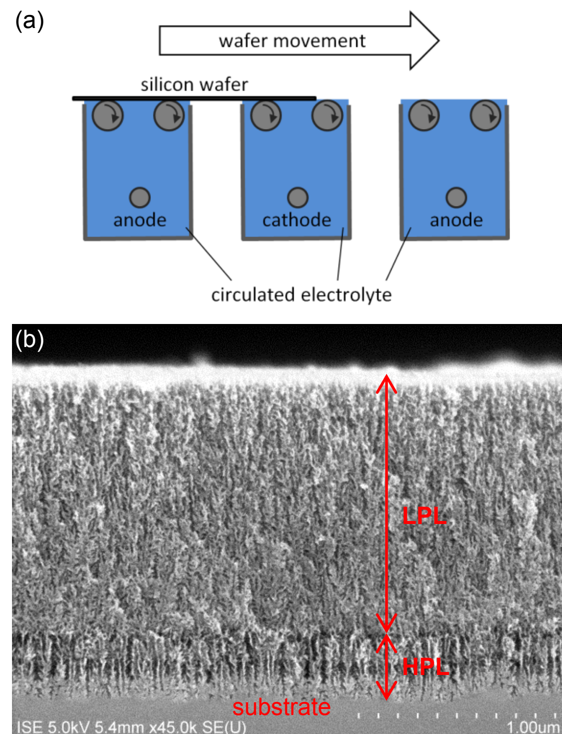

Figure 1: (a) Schematic of the inline porosification tool in a cross-section. (b) SEM image of a cross-section of fabricated porous silicon stack with lowly porous layer (LPL) and highly porous layer (HPL).

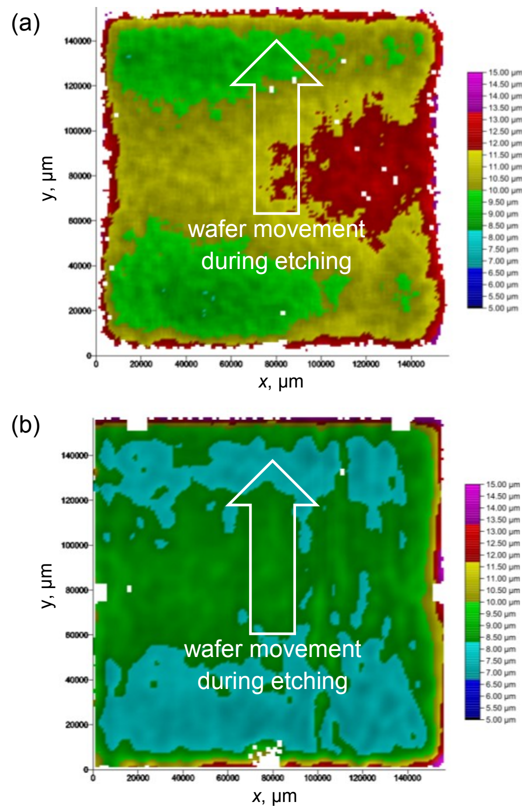

Figure 2: Thickness maps of PorSi layers etched in the inline porosification tool (a) before and (b) after process optimization. For the central region of 136×136 mm^2 the relative standard deviation of thickness is for (a) 9.26 % and for (b) 5.84 %.

electrolyte sink. Wafer movement is realized by rotating rollers. Anodic and cathodic contacts to the wafer are provided on the same wafer side as wet contact to electrolyte. Thus the wafer side facing down (wafer frontside) is porosified while moving over the anodic tank. The setup can be extended with additional tanks for inline etching of multiple layers with different properties in one run. To remove hydrogen bubbles from the etched silicon surface, electrolyte circulation is applied. As electrolyte, a mixture of 49 m% HF, water, and a surfactant was used resulting in approximately 20 m% HF solution. The process was conducted in current-control mode with computer-controlled current sources from Plating Electronic GmbH (Sexau, Germany). Due to limited range of possible wafer movement speed in the tool, lowly porous layer (LPL) of maximum 200–300 nm could be etched per run. To form LPL of total thickness of 1–2 µm, the wafers had to be processed multiple times for several (up to 20) runs to reach the desired thickness. For highly porous layer (HPL), several runs were also applied at higher wafer movement speed for more efficient removal of hydrogen bubbles and safety reasons. After porosification, the wafers were rinsed in deionized water and placed into IPA for 60 s to remove possible rests of surfactant from PorSi and reduce mechanical stress during drying of PorSi.

In order to optimize homogeneity of the inline porosification tool, numerical simulation (FEM) in Comsol 5.3a were conducted.

A cross section, characterized with Scanning Electron Microscopy (SEM) as one representative example of fabricated PorSi stack with LPL and HPL is shown in Figure 1b.

As a reference, wafers (8”) from imec with LPL and HPL were used, which were stored after porosification up to several months and HF-dipped right before further processing.

The porosified Si wafers were reorganized at 1120 °C under 100 % H_2 atmosphere in a high throughput inline CVD tool [5]. The Si epitaxy was done at the same temperature in a chlorosilane / H_2 atmosphere leading to layers of 40–100 µm thickness. The sample doping was realized by inserting diluted PH_3 gas during the epitaxy process.

With a dicing saw the detachment area was defined followed by a lift-off process with a vacuum tool.

2.2 Characterization

Thickness of the wafers before porosification and after epitaxy was measured with CT250T optical thickness measurement device from cyberTECHNOLOGIES GmbH (Eching, Germany). The difference between the thickness measurements showed the thickness of the epitaxial layer. In order to evaluate the homogeneity of PorSi single layers and to optimize the current profile for the etching process, the same characterization procedure has been applied for few wafers with thickness measurement before porosification and after selective removal of PorSi in dilute KOH solution.

After separation, some sample cross-sections have been examined with SEM to examine the reorganization of the porosified template. For preparation of sample cross-sections, cleaving of samples with diamond pen provided sufficiently good results.

3 RESULTS AND DISCUSSION

3.1 Porosification

Due to the inline character of the porosification tool, PorSi layers showed some inhomogeneity. An example of PorSi thickness map with typical types of inhomogeneity is shown in Figure 2.

One type of lateral inhomogeneity results from connection of cathodes to the wafer frontside. Due to charge flowing through the wafer from side tanks to the middle tank, current density is inhomogeneous over the wafer frontside, with current crowding occurring close to the side walls of the anodic tank. Additionally, there is also the wafer movement over the anodic tank. Our electric simulations of the process showed that with simple current profile with ramp up / constant / ramp down parts the central part of the wafer (y in the range 60–100 mm in Figure 2a) gets more total charge density. This results in a thicker PorSi in the middle part of the wafer. With help of FEM simulations, a more complex current profile was developed to partially reduce this effect (s. Figure 2b).

Another source of lateral inhomogeneity of PorSi thickness was the voltage drop in the glossy carbon electrodes connected only from one side to the current source. This resulted in thickness and porosity reduction in x-direction from right to left (s. Figure 2).

The last but not least source of the lateral inhomogeneity in the used inline etching tool is the current crowding at the wafer edges resulting in thicker and less porous PorSi (s. Figure 2). This kind of inhomogeneity (edge effect) is typical for electrochemical setups where the size of workpiece and the tanks with electrodes are not matched. Supported with electric simulations, the edge effect on the wafer edges parallel to wafer movement could be partially reduced by reducing the length of the electrodes in the tanks (s. Figure 2b). Another possible solution could be introduction of additional objects in form of a tunnel or a blind into the anodic tank to modulate current flux. This however could interrupt circulation of electrolyte in the tank thus reducing the removal of hydrogen bubbles from the wafer frontside.

Besides homogeneity of PorSi layers over wafer area, the homogeneity of PorSi layers in depth is also important for correct development of the HPL to a separation gap during reorganization. Due to the movement of wafer during porosification, lateral inhomogeneity of current density results in transversal inhomogeneity of the PorSi layers. In Figure 1b this kind of inhomogeneity helps to distinguish two layers in HPL formed in two runs.

Porosity and thickness of PorSi layers define the degree of reorganization the PorSi layers can get at certain reorganization conditions. Inhomogeneity in PorSi layers make finding optimal process conditions for porosification and reorganization difficult and might reduce yield of EpiFoil detachment dramatically.

While etching PorSi multilayers, the properties of the subsequent PorSi layers (porosity, thickness) depend strongly on the properties of the upper PorSi layers which are etched first. Inhomogeneity of porosification process during etching of LPLs can result in not sufficiently developed or overetched HPLs. In the latter case the PorSi layer might detach during porosification or further processing making growth of homogeneous EpiFoils not possible. For the wafers etched in our inline tool the PorSi lift-off was especially strong on the wafer edges due to the edge effect which made full-area detachment more difficult. That is why wafers in this work were detached in a smaller area.

For formation of a good separation layer during reorganization, it is crucial to have well-defined porosity gradient (e.g. a clear double-layer structure of LPL+HPL) [6]. The transversal inhomogeneity of PorSi layers might make formation of a good separation layer during reorganization difficult. However, transversal inhomogeneities can be used on purpose to form several local separation layers in a kind of puff pastry like structure where detachment of EpiFoil might proceed in any of the separation layers thus increasing yield (s. Figure 3).

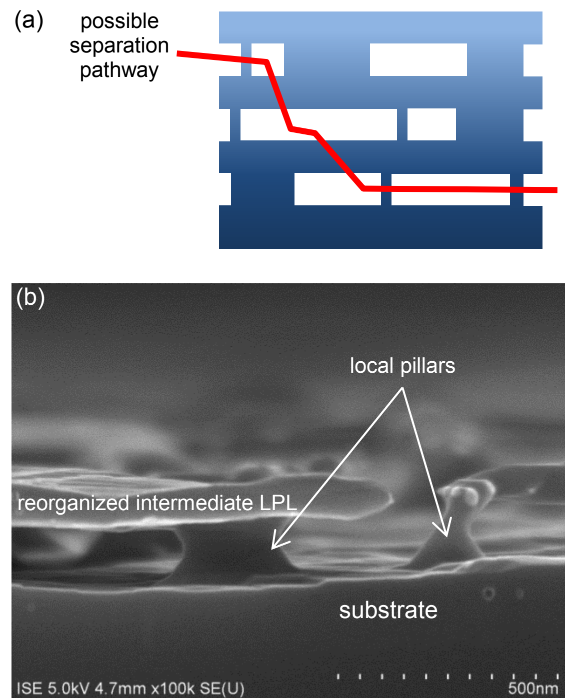

Figure 3: (a) Schematic cross-section of PorSi after reorganization with multiple separation layers. (b) SEM image of a cross-section of PorSi stack with multiple separation layers after reorganization and detachment.

3.2 Reorganization and epitaxy

Reorganized PorSi layers with epitaxially grown Si layer of thickness in the range 40–100 µm were obtained in the inline CVD tool. For test and characterization purposes, also thicker epitaxial layers were fabricated.

For wafers with small number of HPLs, we identified thick interconnections like Si pillars (Figure 4) in the highly porous detachable layer after reorganization as main cause for incomplete or impossible EpiFoil lift-off. Several explanations are possible how these large pillars are built. Two examples of process related issues leading to large remaining interconnections are shown by SEM images in Figure 4.

The first example shows that selective etching [7] of the PorSi during the inline reorganization or too strong reorganization leads to the formation of such interconnections with large cavities in-between (Figure 4a). The formation of large cavities can also be the results of laterally inhomogeneous PorSi layer (s. section 3.1).

To compensate for this inhomogeneity, multiple HPLs were used (s. Figure 3), so that the detachment can proceed along multiple step heights. The drawback of having several separation layers is in possible contamination of the working area with pieces of PorSi layers flowing away from the substrate during the detachment in form of “Si-flakes”. Additionally, PorSi designed for multiple separation layers tends more easy to lift off during porosification or reorganization, thus contaminating the CVD tool and other processed wafers. By applying PorSi layers with multiple LPLs and HPLs with reduced current, and by optimizing the number of HPLs iteratively, we achieved detachable EpiFoils with almost no “Si flakes”.

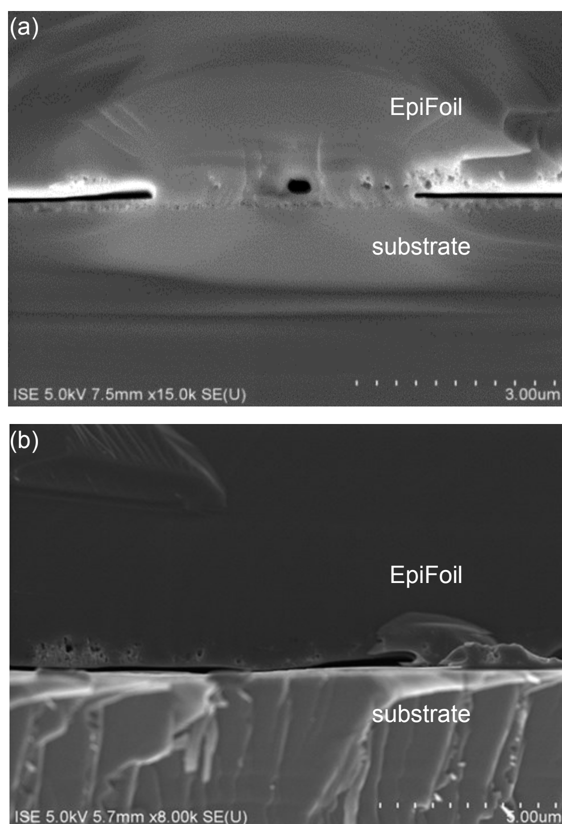

Figure 4: (a) Formation of a large diameter silicon pillar; (b) collapse of the cavity between substrate and epitaxially grown layer.

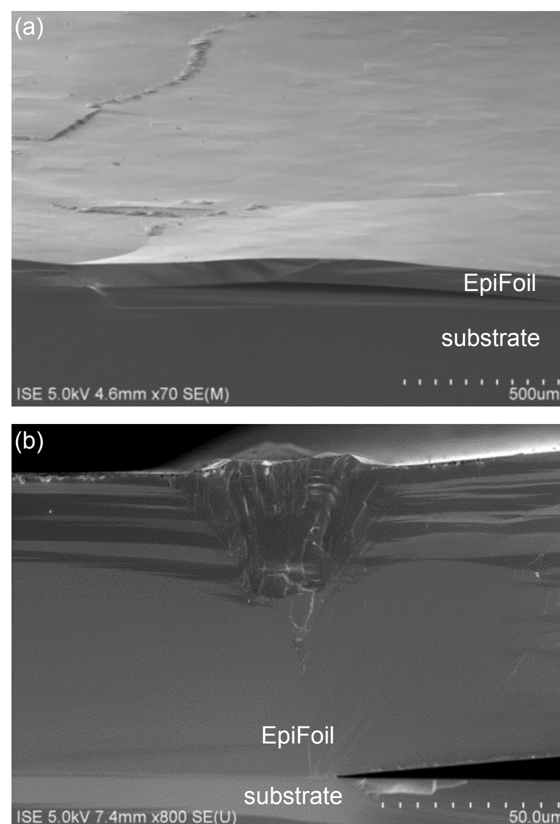

Figure 5: Local warping of the reorganized template leading to (a) sticking of the silicon EpiFoil at the edges of the warped area, and (b) formation of defects (stacking faults).

The second example shows that large cavities without smaller supporting Si pillars can collapse and the EpiFoil can re-attach to the substrate making detachment of this area impossible (s. Figure 4b). Additionally, local warping of the reorganized template before or during epitaxy can lead to detrimental defects like stacking faults (see Figure 5).

The adjustment of etch currents and the numbers of porosification runs for LPL and HPL also helped to offer sufficiently small supporting sites to prevent the collapse of the cavity during the H_2 anneal.

Through an improved process within our inline CVD equipment, selective etching of the upper LPLs through formation of SiO_x during reorganization [7] could be prevented. Although the main task was to improve the detachment yield of large area Si EpiFoils, there are still improvement steps necessary to further increase the quality of the EpiFoils, e.g. effective carrier lifetimes. Since it is known, that the pore size of the surface influences the quality of the reorganized template, a main trigger to increase the lifetime, is to manipulate the surface of the porous Si surface in the porosification process.

3.3 EpiFoil area definition and detachment

The saw dicing and detachment was done in tools with manual wafer handling. However, with state-of-the-art automatic wafer handling solutions, batch dicing and detachment of wafers is possible and already done in microelectronic fabs.

4 CONCLUSIONS

In this paper inline aspects of fabricating freestanding epitaxially grown thin silicon (EpiFoils) for solar cells are discussed. Movement of wafers during porosification introduces lateral and transversal inhomogeneity of PorSi layers which might make formation of good separation layer more difficult. Electric simulations can help to optimize inline porosification process.

One of the solutions to ensure good detachment of the films is to form several local separation layers in a kind of puff pastry like structure where detachment of epitaxial film might proceed in any of the separation layers thus increasing yield.

Improper process conditions during porosification or reorganization might lead to formation of large cavities without smaller supporting silicon pillars, which can collapse during reorganization making detachment of this area impossible. Additionally, this can lead to formation of stacking faults.

Further work has to be done to enhance yield and quality of fabricated EpiFoils.

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