ORIGIN AND IMPACT OF CRYSTALLOGRAPHIC DEFECTS IN EPITAXIALLY GROWN SI WAFERS

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ABSTRACT: In recent years epitaxially grown wafers (EpiWafers) made their way from small laboratory to production scale fabrication. A lot of effort has been put into upscaling of tools, improvement of material quality and in the fabrication of highly efficient solar cells. In this publication we investigate typical crystal defects appearing in EpiWafer material and correlate them with process or reactor specific features like porous templates, thick epitaxial layer growth or inline processing. We find two categories of stacking faults (SFs) which are either decorated with inclusions or not. Besides particles on the surface of the growth template contaminations with oxygen are found to be reasons for such polycrystalline inclusions. Stress leads to either delamination of the template or local lattice strain both reasons for defect growth. Parallel faults which propagate along slipping lines in the material are interacting with SFs although the correlation is not fully understood yet. Finally the recombination activity in SFs is found to be especially high where the {111} planes meet or when strong decorating occurs. This work is a first step to systematically investigate the crystallographic nature of EpiWafer material and will help to further improve processes and equipment.
Keywords: Silicon, EpiWafer, defects, kerf-less wafering, stacking faults

1 INTRODUCTION

Efficiency improvement and reduced consumption of resources are main drivers for today's PV developments. Epitaxially grown silicon wafers "EpiWafers", prepared by detachment of the silicon layer grown epitaxially on a reorganized porous silicon template, offer the possibility to reduce silicon and energy consumption and with this production costs while maintaining high efficiency potential. In recent years a lot of effort has been put in the development of equipment capable of high-throughput and low cost production in order to enable a technology transfer from semiconductor to photovoltaic industry. Today the EpiWafer is on its way to become a cost-efficient alternative for standard mono-crystalline wafers in photovoltaic applications[1]. Besides the significant progress in industrialisation of the EpiWafer technology several solar cell concepts have been successfully applied to this new material [1], [2]. However, although some research groups report on the necessity of post-treatments like gettering to exploit the full electrical potential of the epitaxially grown wafers [3], [4] systematic studies about specific defects and their origin are completely missing so far. In this publication we try to close this gap with the analysis of defects which we find in EpiWafer material and compare them to known defects in epitaxially grown Si from literature. Almost all available publications on related subjects so far focus on epitaxy on standard wafers and epitaxial layer thicknesses of below 100 µm. Only recently the interest in Si epitaxy of layers beyond 100 µm thickness used for power devices has been raised again [5]. However, so far we could not find any literature about epitaxially grown Si layers with thicknesses exceeding 100 µm grown on porous Si templates. Besides that many publications do not clearly indicate how the EpiWafers were fabricated (reactor and process details) and crystallographic information like stacking fault and etch pit density are simply missing. In this work we explain in detail how the EpiWafers have been processed, identify different classes of defects, investigate their origin in the course of the fabrication process and characterize their influence on the electrical quality of the material.

2 EXPERIMENTAL

The porosified 6-inch Cz samples for all experiments have been prepared by the Institute for Microelectronics in Stuttgart (IMS) featuring a low porosity layer on top of two high porosity layers. All wafers were cut to 10 cm edge length on one side and were cleaned in aqueous hydrofluoric acid (HF) with a concentration of 1 % before mounting in the quasi-inline RTCVD 160 furnace [6]. The reorganization processes took place at a peak temperature of 1150 °C under 100 % hydrogen atmosphere for up to 30 min. Subsequently the quasi-inline Si epitaxy process was done at the same temperature in trichlorosilane (TCS) / H_2 atmosphere with a Cl / H gas flow ratio of 12 % and process times of 80 min to achieve layer thicknesses of 150 to 200 µm. For the n-type samples the PH_3 flow was set to achieve a constant layer doping of approximately 3E15 cm^{-3}, which is a quite common value for highly efficient wafer solar cells. Some samples were just reorganized and measured afterwards with Secondary Ion Mass Spectroscopy (SIMS) at RTG Mikroanalyse GmbH to determine oxygen concentrations throughout the porous silicon layer stack. Therefore the reorganized samples were broken just before loading into the SIMS chamber in order to avoid any native oxide growth inside the porous Si structure which could distort the measurement.

Cross sections were prepared with simple sample cleaving and investigated with Scanning Electron Microscopy (SEM) and an in-situ Energy Dispersive X-ray spectrometry (EDX) setup. Before scanning the surface with an optical microscope the samples were etched in SECCO[2] solution to visualize defects. From these images stacking fault distributions were derived.

Prior to detachment 5x5 cm² areas were defined on the wafers using a dicing saw from DISCO. We detached the EpiWafers in an in-house developed lifting tool

[1] www.nexwafe.com

[2] SECCO-etch: HF + $K_2Cr_2O_7$ + H_2O in a ratio of HF : H_2O = 2 : 1 with 44 g $K_2Cr_2O_7$ dissolved in 1 l of H_2O.

which basically provides homogeneous soaking through special membrane materials over defined sample areas. The residual porous and highly doped Si layer was etched in a CP71 wet chemical bath with an etching rate of around 1.4 µm/min for around 3 min. Both sides of all samples for electrical characterization were passivated in an Atomic Layer Deposition (ALD) tool with 20 nm of Al_2O_3. The spatially resolved measurement of minority carrier lifetimes was done using micro-photoluminescence (µPL) [7].

3 RESULTS AND DISCUSSION

The first inspection of the surface with microscopy shows squared shaped stacking faults with shiny and dark surfaces. This difference in reflection originates from the surface structure which is (i) completely flat and in the same plain as the surrounding epitaxial layer for the shiny regions and (ii) coming out of the plain and structured for the dark ones. We call the shiny ones non-decorated and dark ones decorated SFs. It is known from literature that in general SFs arise from atomic defects. They originate from small mismatch between first growth area with respect to the substrate, are therefore initiated at the substrate / layer interface and grow along inclined {111} planes [8]. On a (100) oriented substrates there are four such planes which are tilted by 54.7° (in relation to the surface) leading to a squared shape structure at the intersect with the surface. If just one of such a pyramidal structure is occurring and no additional defects arise in the proximity of the SF we call it a non-decorated SF. These kinds of SFs are readily found in epitaxially grown Si layers on Si substrates. In the following we focus on decorated stacking faults and try to give some explanations for their origins especially linked to the reorganized porous layer stack which is used for EpiWafers as growth template.

3.1 Particles and oxygen background

Some of the SFs show poly crystalline inclusions of which some have their origin in particles located at the substrate / layer interface. In Fig.1 one such particle can be found in the SEM micrograph of a respective cross section. Several twin grain boundaries, intercepting crystal planes and the non-oriented structures coming out of the surface plain show the high degree of decoration. EDX measurements presented here (Fig.1, right) identify quartz particles which can be explained by carrier abrasion during movement of the samples. Besides movement related to abrasion at reactor components which are made of e.g. quartz or coated graphites, particles can also arise from gas phase nucleation or parasitic depositions on the reactor walls and then fall on the growth template. Moreover the handling of porosified wafers can be another source of particles or scratches which can influence not just the epitaxial growth but the reorganization process itself.

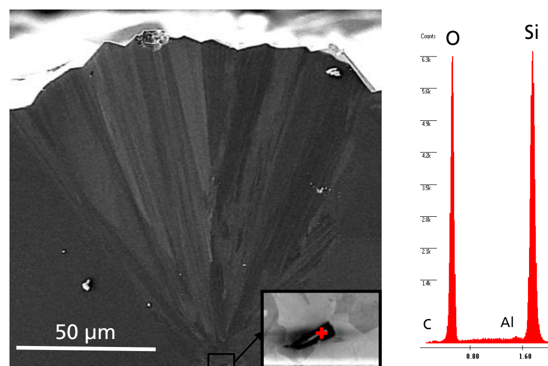

Figure 1: SEM micrograph of a cross section showing a decorated stacking fault (left) with an included particle (inset). EDX data measured at particle position (right) showing high oxygen concentrations which suggest a quartz particle.

Contaminations at the growth template can be another reason for the decoration of SFs. Especially metals and oxygen are known to cause such defects in epitaxially grown Si layers on even crystallographically perfect Si substrates [9]. Ravi *et al.* [10] report that C concentrations of E19 at./cm^3 already lead to SF growth. On the reorganized porous layers the gettering effect caused by the large internal Si surface [11] has to be considered. All impurities which are already present in the parent substrate or in the reactor ambient during reorganization are gettered and can lead to locally very high e.g. metal concentrations. Pomerantz *et al.* [12] report that high contamination levels of metals such as Cu, Fe, Ni and others lead to precipitates which are nucleation sites for SF growth. Although no such precipitates could be found we still consider metal impurities as one important origin of crystal defects. For one there are many sources of metal contaminants inside the reactor and gettering of EpiWafers shows significant improvement in minority carrier lifetime [3].

In order to investigate the oxygen concentration in the reorganized porous layer and on its surface we measured such structures with SIMS after hydrogen processing (reorganization). In Fig.2 the SIMS profile from seed wafer to surface (right to left) shows oxygen concentration of up to E21 atoms cm^{-3} in the porous layer. An unwanted oxidation of samples during preparation can be excluded as all samples were broken directly before transferring them to the SIMS chamber. The concentration at the surface is lower than in the porous bulk (E20 atoms cm^{-3}) and shows a strong dip close to the transition zone between these two. Besides the native oxide growth during shipment, which could not be prevented, the signal accuracy in the first nanometers of the profile is questionable. We therefore cannot finally conclude on the real oxygen concentration on the template. However, as the concentration inside the porous structure is very high oxygen is supposed to play a role in the first layers of Si growth. Finch *et al.* [13] report that oxide can produce steps at the surface forcing the silicon crystal to grow around such an oxide inclusion leading to the formation of stacking faults.

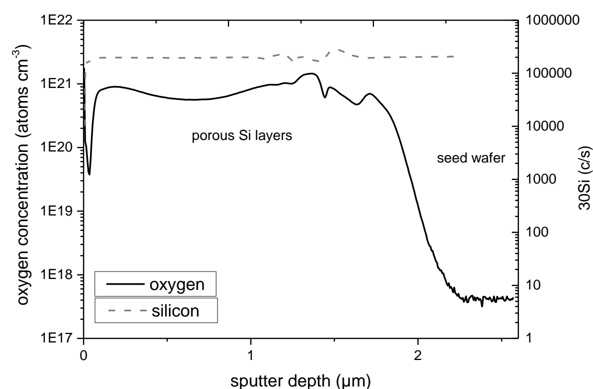

Figure 2: SIMS measurement through porous Si layers into seed wafer after reorganization showing oxygen (solid line) and silicon (dashed line) content.

3.2 Stress and template

Other reasons for defects in epitaxially grown layers can arise from structural or crystal imperfections of the template. Such imperfections can be e.g. not fully reorganized templates containing holes or uneven surfaces [14]. However, even a smooth template is strained due to stress between the seed wafer and the porous layer. In certain cases the strain can be such high that a delamination occurs. In Fig.3 the cross section of an epitaxial layer on a partly delaminated porous layer stack is shown. Originating from the delaminated part of the template a defect rich crystal growth is visible. Surprisingly the left part of the SF seems to be mainly unharmed which leads to a non-symmetric shape of the SF. We call this a partly decorated SF.

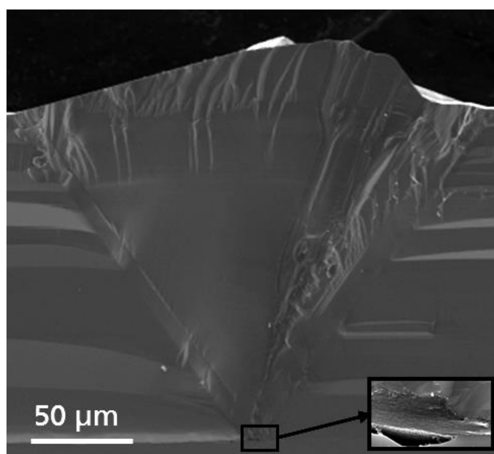

Figure 3: SEM micrograph of a cross section showing a partly decorated stacking fault with a locally detached porous Si layer stack (inset) being the origin of the polycrystalline growth.

Besides this macroscopic effect of strain on the crystal growth a more microscopic effect has to be considered. In an energetically optimized state all pores should be either spherically shaped or oriented along crystallographically preferred planes. Due to limited energy / time during reorganization and / or residual oxygen on the pore's inner surfaces preventing defect diffusion not a single such perfect pore can be found. However, the pores in proximity to the surface show additional deformations (see Fig.4, left) which look like a flattening. During reorganization the Si atoms are looking for energetically preferential sites which leads to dissolving of small pores or the growth of the larger ones [15]. The templates surface is a pore with infinite size which means that Si atoms want to diffuse there. On the other hand pores in proximity of it tend to close their surface as it is energetically preferential for them. These competition leads to the flattening of the pores which is an energetic compromise leading to microscopic lattice strains in such areas. After epitaxy this strained areas can be identified as the origin for several close parallel faults which grow in the direction on the {111} plane (Fig.4, right).

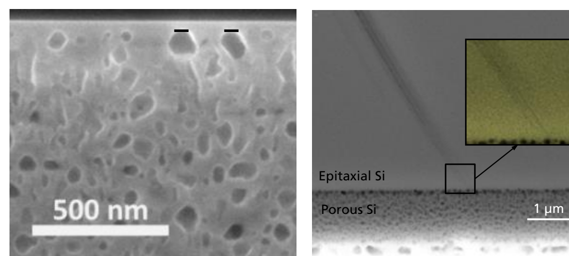

Figure 4: SEM micrograph of cross section showing a reorganized porous layer with flattened pores in close proximity to the growth template (left) and parallel faults originating from one of such pores (right).

During epitaxy the generated mismatch is compensated through these close parallel faults. In Fig.5 (left) one example for such an accumulation of defects on the fringes of a SF is shown in cross section view. Several variations with an increasing number of close parallel faults can be found in the EpiWafer material. The number of additional growth planes could be explained by different strain levels leading to increased mismatch between crystal structure of template and growing layer. In Fig.5 (right) top views of intersects of the {111} planes with the surface are shown. The increasing number of parallel faults (counterclockwise) caused by increased mismatch / strain leads to pyramidal structures with increasing height.

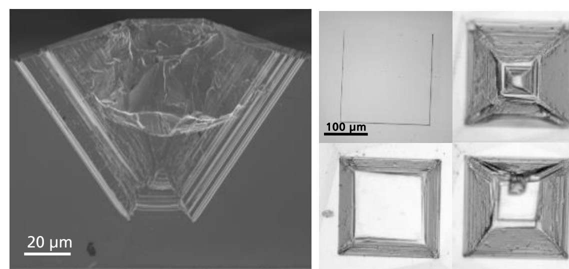

Figure 5: SEM micrograph of defect etched cross section showing close parallel faults along the {111} planes (left). Top view (microscope) of epitaxially grown layers with increasing number of parallel faults (right, counterclockwise).

3.3 Effect of stacking faults on electrical quality of the EpiWafer

In a first step we identified SFs without and with polycrystalline inclusions (decorated SF) in an optical microscope. On the same spot non-calibrated µPL measurements were performed. In Fig.6 the microscope pictures (top) show a non-decorated SF (left), a SF with some parallel faults (middle) and one filled with polycrystalline inclusions (right). The corresponding

lifetime mappings for the first two show cross like features identifying highly recombination active regions. These cross like shapes overlap with the intersects of the {111} planes which are partial dislocations extending from the nucleation to the surface. It is not surprising though that these regions show enhanced recombination activity. The fully decorated SF seems to be highly recombination active throughout its whole volume. It is not clear so far for all these defects if the decoration with contaminants such as metals or dangling bonds / vacancies is the reason for the high recombination activity.

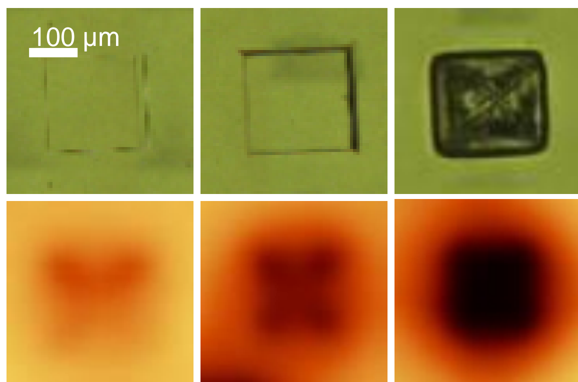

Figure 6: Microscope pictures of top view on epitaxial Si layer (top) and µPL mapping of corresponding regions (bottom).

When looking at µPL mappings of larger areas of the EpiWafer we find regions with enhanced recombination (black) following exactly the family of directions <110> (see Fig.7). Obviously these lines correspond to another crystal defect. Considering their orientation we conclude that these are line defects which glide along slip planes of the crystal. It is known that such defects occur when the temperature gradient along the wafer is in the range of 5 – 10 K cm^{-1} [16] at growth temperature. In most cases they start at wafer edges initiated by little damages. In our case we find that most line defects intersect with SFs. Especially at the crossing points of such slip lines the highly recombination active (decorated) SFs can be found. We came up with two explanations for these effects: (i) After growing an epitaxial layer of 150 µm and more the EpiWafer is exposed to a temperature gradient exceeding 5 – 10 K/cm which initiates parallel faults at existing SFs which then glide to the fringes of the wafer. (ii) During reorganization parallel faults are generated again due to thermal process inhomogeneities at micro stress regions in the porous layer itself and glide then along slip lines through the whole template. At the crossings of such line defects step like surfaces can lead to SF growth due to lattice mismatch.

Ravi *et al.* [10] find this effect on (111) wafers although without any porous layer involvement. Arguments that several crossings can be found where there is no SF visible support theory (i). Unfortunately there are not many µPL mappings available showing such features. Furthermore these mappings are limited in terms of spatial resolution which makes it difficult to verify such arguments.

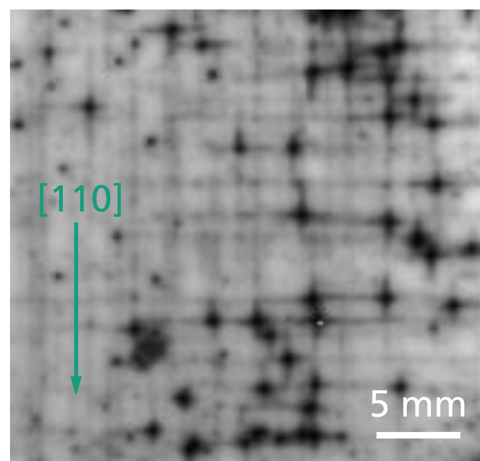

Figure 7: PL image of an EpiWafer after detachment showing SF and line defects as highly recombination active areas in black.

At the moment we can conclude that there are good arguments for both hypotheses and that further investigations using defect etching on just reorganized samples looking for initial parallel faults and µPL images with higher resolution will be necessary to finally understand the relation between parallel faults and SFs.

4 CONCLUSIONS

We identify stacking faults (SFs) with and without poly crystalline inclusions as the most detrimental crystallographic defects in EpiWafers. Decorations within such SFs seem to be initiated by either inclusions like quartz particles from the sample holder or by delamination of the porous Si layers. SIMS measurements reveal oxygen (≈1E21 at/cm^3) on the reorganized Si template as another reason for the appearance of SFs. Macroscopic and microscopic stress influences the template and can lead to delamination, a strained lattice or parallel faults throughout the whole wafer. µPL reveals that especially decorated SFs are highly recombination active which can be explained by the high concentration of defects and grain boundaries.

Although several reasons for crystal defects like metal contamination or high dopant concentration on the growth template could not be investigated and the role and origin of stress is not fully understood yet our investigations will already help to further improve the material quality and to understand related effects in the solar cells' performance like e.g. decreased fill factors and others.

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