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SPUTTER DAMAGE TO AMORPHOUS SILICON LAYERS FOR HETEROJUNCTION SOLAR CELLS

Britt-Marie Meiners, Sven Holinski, Petra Schäfer, Stefan Hohage, Dietmar Borchert
Fraunhofer Institute for Solar Energy Systems, Laboratory- and Servicecenter Gelsenkirchen, Auf der Reihe 2, 45884 Gelsenkirchen, Germany, phone: +49 209 155 3922, fax: +49 209 12090 93

ABSTRACT: High-efficiency silicon solar cells, like the silicon heterojunction cell with thin intrinsic layers (HIT) [1, 2], use transparent conductive oxides (TCO) as anti-reflection layers. The production of these layers using sputtering technology can cause damage to the underlying layers. This damage can be seen in a degradation of the surface passivation properties. With the help of various protections against different damage causes we analyzed the origin of the sputter damage. We also investigated the different degradation behavior of single layer intrinsic amorphous silicon layers ((i) a-Si) and p/n-doped silicon layers on top of intrinsic amorphous silicon layers as stacks. The influence of the intrinsic passivation layer thickness on the amount of degradation was also investigated. The results show that a doped layer can protect the intrinsic layer from sputter damage. The damage itself is caused by plasma photons in the range of 2.5 to 4.15 eV.

Keywords: Heterojunction, TCO, Passivation, Degradation, Sputter

1 INTRODUCTION

The excellent surface passivation of amorphous silicon layers is an important parameter for high-efficiency silicon heterojunction solar cells [3, 4]. To identify a cause of the degradation of the surface passivation by sputtering helps to better understand the deposition process and to improve the cell efficiency [5, 6]. So the sputter process parameters can not only be chosen for specific TCO attributes but also for a deposition process which causes a reduced amount of degradation. Our investigations lead to a better understanding of the interaction of the different process steps during the production of heterojunction solar cells. It helps to optimize the production of solar cells and to treat the underlying layers with care when there is a process step which could damage these.

In our experiments the (i) a-Si passivation layer was deposited on both sides of high quality textured float zone wafers. On one side an additional doped layer was applied. Onto this side the indium tin oxide was sputtered. In order to gauge the degradation of the surface passivation effective lifetime measurements by µPCD were done on the samples before the sputter process, after the sputter process and after an annealing step.

2 EXPERIMENTAL

RCA cleaned textured float zone wafers with a 3 Ω base resistance were passivated on both sides with intrinsic amorphous silicon after a 3 minute dip in 1 % HF solution.

The doped amorphous silicon layers, as well as the intrinsic layers, were made by plasma enhanced chemical vapor deposition (PECVD). While the intrinsic layers were deposited on both sides of the wafer, the doped layers were only deposited on one side of it.

The thickness of the single intrinsic layers varies from 10 nm over 20 nm to 36 nm. For the i/p stack the thickness is 10 nm for the i-layer and 5 nm for the p-doped layer respectively. The i-layer for the i/n stack has the same thickness whereas the n-doped layer is 10 nm thick.

Only one side of the wafer is coated with a 78 nm thick indium tin oxide (ITO) by sputtering. The ITO for the wafers with the intrinsic/doped stack was deposited on the side with the stack. All sputter processes had the same working pressure (1.6E-3 mbar), gas mixture (2 % O_2) and power density (1.1 W/cm²). The RF process differs in the power density (1.6 W/cm²) and the gas mixture (non-reactive).

The sputtered ITO was etched away using an HCl solution. The effective lifetime of the samples were measured with µPCD (microwave photoconduction decay) before sputtering after the etching step and after an annealing step. The annealing step was carried out in air at 150 °C for 12 minutes on a hotplate. For the protection against the sputter damage a glass and a foil with different transmission properties were used on top of the sample surface during the sputter process.

For the light degradation on the 10 nm (i) a-Si passivated wafer a solar simulator together with different light filters was used. The duration of the irradiation was proportionately adjusted.

3 RESULTS

3.1 Thickness dependent degradation

In figure 1 the effect of the intrinsic layer thickness on the surface passivation degradation by different processes is shown through relative changes of the effective carrier lifetime.

$$\frac{\Delta\tau}{\tau} = \frac{\tau - \tau_{after}}{\tau}$$

Here τ is the lifetime before degradation and τ_{after} the lifetime after degradation or after annealing.

There is no difference in the effective lifetime changes between the various sputter processes with and without ex-situ annealing when the layer is only 10 nm thick. This is different for higher thicknesses. For the 20 nm thick film the process with the higher (150 °C) substrate temperature (blue symbols) causes less degradation than the process without extra heating (black symbols). Both lifetime changes can be reduced by an ex-situ annealing step. The same behavior is observed for a film with a thickness of 36 nm. The difference in degradation between 36 nm and 20 nm is less than the difference between 10 nm and 20 nm.

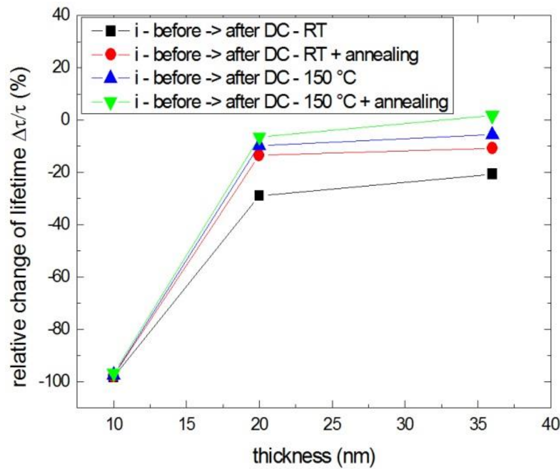

Figure 1: Relative change of the effective lifetime depending on the intrinsic amorphous film thickness for DC sputtering at two different temperatures

3.2 Process dependent degradation

In figure 2 the decline in lifetime for different substrate temperatures during the DC sputtering process is shown. Here a clear distinction between the single layer, the i/p (10 nm/5 nm) and the i/n stack (10 nm/10 nm) is visible. The degradation of the single layer does not depend on the substrate temperature. In general the i/p and the i/n stack show the same trend with increasing temperature: the degradation decreases. The only exception is the degradation of the i/p stack after annealing (purple symbols). A decrease in lifetime with increasing substrate temperature can be observed.

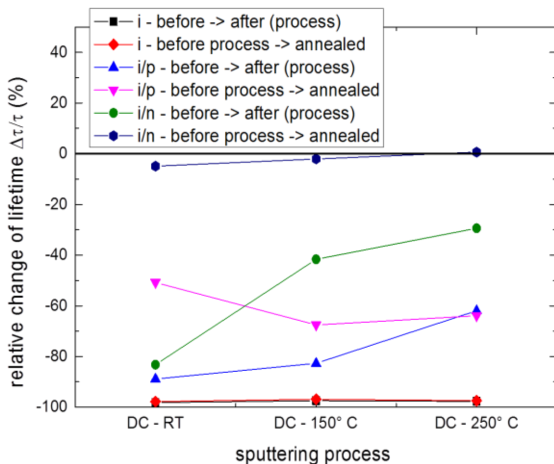

Figure 2: Change of the effective lifetime depending on the DC sputtering process temperature for different layer systems

In figure 3 the difference between damage caused by the RF sputter process and by the DC sputter process at 250 °C is shown. For the intrinsic single layer no clear difference is recognizable. While the degradation of the i/n stack increases, the degradation of the i/p stack slightly decreases as shown by the lifetime changes.

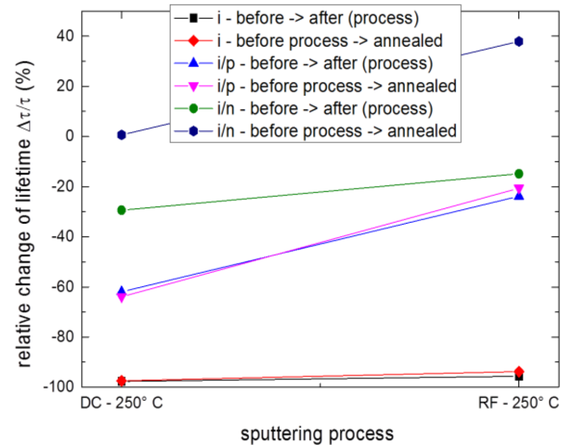

Figure 3: Change of the effective lifetime between RF and DC sputtering processes at 250 °C for different layer systems

3.3 Cause of degradation

The experiments with various protections (glass and foil) result in the explanation that the cause of sputter damage cannot be ion bombardment or x-rays. Most of the degradation is still present after the glass protected the passivated wafer. Due to the different transmission of the glass and foil, the passivated wafer show a different amount of degradation. Therefor the plasma photons which can explain the caused degradation are in the range of 2.4 eV and higher [5, 6].

In figure 4 the transmission of a (i) a-Si film for different film thicknesses is shown. The same exponential trend can be found in the relative lifetime change for the DC sputtering process without in-situ annealing. This supports that the plasma photons cause the degradation.

The photons cause the degradation through damage to the interface between the crystalline and the amorphous silicon. With thicker passivation layers less photons reach the interface to damage it. This explains the exponential trend in the relative lifetime change for higher layer thicknesses.

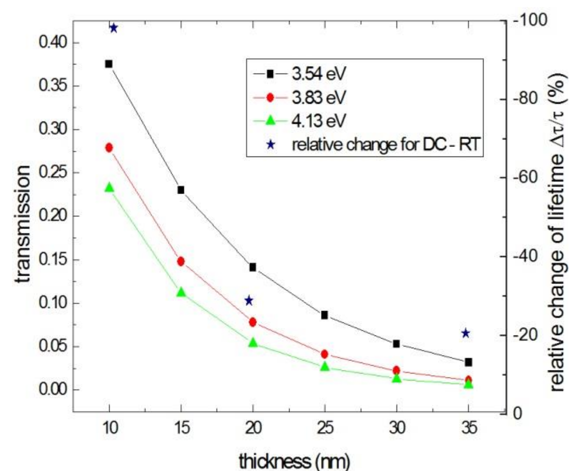

Figure 4: Transmission of a (i) a-Si film depending on the film thickness for different wavelengths (lines and symbols) and the relative change in lifetime for the DC-RT process without ex-situ annealing (stars).

3.4 Light induced degradation

In figure 5 the absorption coefficient for intrinsic amorphous silicon depending on the photon energy is shown.

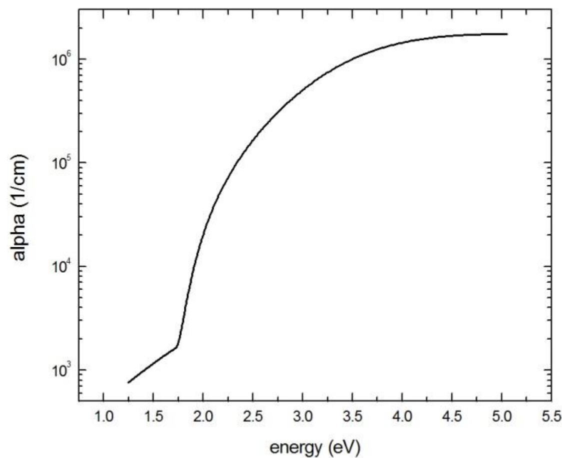

Figure 5: Absorption coefficient for (i)a-Si

There is a steep increase in the absorption coefficient for 2.4 – 3.5 eV and only a slight increase for 3.5 - 5 eV. Therefor more photons with lower energy reach the interface.

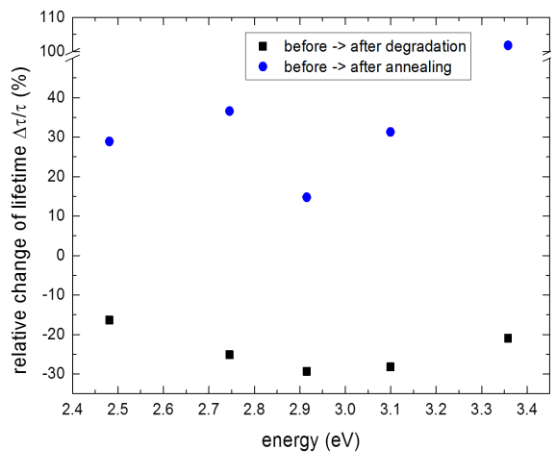

Figure 6: Change of the effective lifetime depending on the energy of the photons

The results of the light induced degradation are shown in figure 6. The initial degradation (black squares) increases when the photons have more energy. For photon energies higher than 2.9 eV there seems to be a decline in the degradation of the lifetime. This can be explained through the steep increase of the (i) a-Si absorption coeffient for photons with higher energy, therefor less photons reach the crystalline/amorphous silicon interface to damage it. For energies higher than 3.5 eV the absorption coefficent increases only sligthly. So the damage to the interface should increase again.

For the light induced degradation the annealing step heals all damage to the passivation and even improves lifetime.

4 SUMMARY

Cause of the carrier lifetime degradation during sputter processes are the plasma photons in the range of 2.5 eV to 4.15 eV. The damage can partly be healed by an in-situ or and ex-situ annealing step. The efficiency of the healing as well as the initial degradation depends on the (i)a-Si single layer thickness, the doping of the protection layer in a stack and the chosen deposition process.

5 ACKNOWLEDGEMENT

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