## INLINE PROCESSES FOR THE STABILIZATION OF *P*-TYPE CRYSTALLINE SI SOLAR CELLS AGAINST POTENTIAL-INDUCED DEGRADATION

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**ABSTRACT:** In order to stabilize multicrystalline Si solar cells against potential-induced degradation of the shunting type (PID-s), an intermediate SiO<sub>2</sub> layer was grown between the  $n^+$ -diffused emitter and the PECVD SiN antireflection coating. Two inline processes were investigated and implemented in an industrial processing sequence: UV oxidation and thermal oxidation in a walking-string furnace. In both cases excellent PID-s resistivity was obtained as measured by a PID-s cell test before encapsulation. After encapsulation in standard glass / ethylene vinyl acetate / backsheet modules the UV oxidized cells exceed the requirements defined in the new edition of the IEC 62804 standard with respect to PID-s resistivity on module level. The thermally oxidized cells are even more stable. Additionally, before PID-s an increase of cell efficiency by 0.2% relative compared to cells without oxide was obtained for thermal SiO<sub>2</sub> films.

Keywords: Degradation, Reliability, Performance

#### 1. INTRODUCTION

In state-of-the-art photovoltaic systems crystalline silicon solar cells are often operated at high negative bias voltage relative to the modules' mounting. If SiN-coated ptype c-Si cells are encapsulated in standard modules, under some circumstances very low shunt resistances arise which reduce the electrical module power close to zero [1,2]. This effect, called 'potential-induced degradation of the shunting type (PID-s)', was recently found to be spatially associated to Na decorated structural defects within the pnjunction of the cells [3,4]. Several solutions exist to avoid PID-s on system, module and cell level. However, an assessment of these solutions revealed that there is a great demand for PID-s free cells because of specific technology and cost constraints for modules and systems [5]. Basically, PID-s stabilized cells can be obtained by modifications of the emitter and/or the SiN antireflection coating. As far as industrial-type emitters are concerned, the modification of the emitter diffusion has only a relatively low impact on PID-s but a big effect on cell efficiency. In order to develop methods for PID-s avoidance independent of the cells' emitter design, we focused on the investigation of very thin SiO<sub>2</sub> films grown on the emitter before SiN antireflection coating (ARC) deposition.

In a recent publication H. Mehlich et al. already reported, that a native oxide grown for 1 h and a thermal oxide grown at unpublished conditions reduce PID-s [6]. Furthermore, excellent PID-s resistivity was obtained by a new surface pre-treatment called SQi but the technology wasn't disclosed at that time. Moreover, in the publication no results were presented on the impact on cell efficiency before PID-s. By now it is stated in [7] that SQi is an ultraviolet-light treatment and an efficiency gain of up to 0.2% absolute can be obtained. Another group studied 7 to 10 nm thick thermal SiO<sub>2</sub> films grown on ion implanted or POCl<sub>3</sub>diffused emitters [8]. PID-s was effectively diminished, but the efficiency of the POCl<sub>3</sub>-diffused cells decreased by 0.7% relative due to inferior front surface passivation of the SiO<sub>2</sub>. For the ion implanted cells no comparison was made between the cell efficiencies with and without SiO<sub>2</sub>.

In this work we investigated two different inline processes for the growth of thin  $SiO_2$  interlayers in order to avoid PID-s: i) oxidation by means of an ultraviolet (UV) lamp at room temperature and ii) oxidation in an infrared (IR) heated walking-string furnace. Since treatment times are short, both processes are well suited for mass production. Additionally, the UV lamp's footprint is very small and hence many existing production lines can be retrofitted with it.

#### 2. EXPERIMENT

Multicrystalline (mc) Si solar cells with the dimensions 156 x 156 x 0.17 mm<sup>3</sup> and a specific base resistivity between 0.5 and 2 Ωcm were manufactured by the following industrial inline processing sequence: After isotexture und clean, a H<sub>3</sub>PO<sub>4</sub> based solution was sprayed on the front side of the wafers. In a thermal treatment the H<sub>3</sub>PO<sub>4</sub> liquid layer was transformed to a solid phosphorous silicate glass (PSG) which served as a dopant source for the subsequent  $n^+$ -diffusion at temperatures between 800 and 900°C. The pn-isolation was performed by rear side etching in diluted HF/HNO<sub>3</sub> and the PSG was removed in HF. After emitter dead-layer etch in an alkaline solution a thin SiO<sub>2</sub> film was grown as described in Section 3 below. The cells were completed by inline plasma-enhanced chemical vapour deposition of a SiN antireflection coating on the front side, screen printing of a large-area Al contact and small Ag solder pads on the rear side, screen printing of an Ag contact grid on the front side and firing. A schematic crosssectional view of the manufactured cells is shown in Fig. 1.

We investigated PID-s of non-encapsulated cells by means of an accelerated cell test. A schematic drawing of the setup is depicted in Fig. 2. It is similar to the setups described in [9,10,11]. The solar cells were placed on a stainless steel plate and covered with a flexible conductive



**Fig. 1:** Schematic cross-sectional view of the investigated multicrystalline Si solar cells.



Fig. 2: Schematic cross-sectional drawing of the setup used for accelerated PID-s tests of solar cells.



**Fig. 3:** Measured correlation between the normalised change of the cell efficiency and the shunt resistance after PID-s.

polymer sheet plus a second steel plate. This stack was pressed together, heated to 75°C and a voltage of 6.5 kV was applied between the steel plates for three hours. The polymer sheet does not stick to the cells and hence the stack could be easily disassembled after the test. Finally, the shunt resistance  $R_p$  and the efficiency  $\eta$  of the cells were measured and compared to the values obtained before degradation.

A plot of the measured normalised change of the cell efficiency  $\Delta \eta/\eta = (\eta_{\text{before PID}} - \eta_{\text{after PID}}) / \eta_{\text{before PID}}$  as a function of  $R_{\text{p.after PID}}$  shows a good correlation, see Fig. 3. Note, that this correlation is valid under the prereqisites of i)  $R_{\text{p.before PID}} >> R_{\text{p.after PID}}$  and ii) the series resistances of the cells are similar. In general, cells that are made on high-throughput machines regularly meet both conditions. It can be seen from the graph, that  $R_{\text{p.after PID}}$  is a more sensitive measure for the PID-s resistivity than  $\Delta \eta/\eta$  if the cells are relatively stable, i. e.  $\Delta \eta/\eta < 1\%$  and  $R_{\text{p.after PID}} > 5 \text{ k}\Omega\text{cm}^2$ . For this reason we discuss the measured distributions of  $R_{\text{p.after PID}}$  rather than that of  $\Delta \eta/\eta$  in section 4 below.  $\Delta \eta/\eta$  key data are also given there.

We conducted a PID-s test on photovoltaic modules as well. For this, standard PV modules with the dimensions 1 x  $1.6 \text{ m}^2$  were manufactured out of 60 cells each. The cross-sectional construction was soda-lime glass / ethylene

vinyl acetate (EVA) / cells / EVA / polymer backsheet. The PID-s test was carried out with an Al foil on the glass surface at a constant temperature of  $85^{\circ}$ C. A voltage of 2000 V was applied between cell matrix (minus pole) and Al foil (plus pole) for 9 days. In intervals of 3 days *IV* curves of the modules were measured at standard test conditions according to IEC60904-1 ( $25^{\circ}$ C, 1000 W/m<sup>2</sup>, AM1.5G) by means of a commercially available flasher.

# GROWTH OF SIO<sub>2</sub> FILMS UV oxidation

The UV lamp was installed above a 5-lane inline wafer transport system consisting of sequenced rollers, see Fig. 4. The lamp is located in front of a robot that loads the wafers on the trays of a horizontal PECVD SiN deposition system (not visible in this view). The UV light is generated by up to 4 mercury-vapour low-pressure discharge tubes which are positioned a few centimetres above the Si wafers. The discharge tubes are made highly UV-transparent fused quartz. The mercury vapour emits a characteristic line spectrum with strong peaks at wavelengths of 185 nm and 254 nm in the UVC spectral range, see Fig. 5 [12]. At a wavelength of 185 nm the UV radiation produces atomic



**Fig. 4:** Photo taken from the UV lamp installed above a 5lane inline wafer transport system. For clear visibility of the inner structure the gas discharge tubes were turned off and the front cover of the housing was removed.



**Fig. 5:** Typical spectrum of the used mercury-vapour low-pressure discharge tubes [12].

oxygen and ozone from the molecular oxygen in the ambient air according to the reactions [13]

(1)  $O_2 + hv \rightarrow 2 O \quad (\lambda = 185 \text{ nm})$ 

(2) 
$$O + O_2 \rightarrow O_3$$
.

The atomic oxygen reacts with Si

$$(3) \qquad 2 O + Si \rightarrow SiO_2$$

and the ozone acts as a supplier of atomic oxygen:

$$(4) \qquad O_3 + O_2 \rightarrow 2 O_2 + O$$

(5)  $O_3 + hv \rightarrow O_2 + O \quad (\lambda = 254 \text{ nm}).$ 

The maximum ozone concentration measured at wafer transport level was 28 ppmv. It must also be noted that the Si wafers moderately heat up to about 35°C under irradiation.

The photo shown in Fig. 4 was taken after removal of the housing's front cover in order to show the lamp's inner structure. In normal mode the front cover protects the operator from ozone and UV radiation and the wafers enter and leave the lamp via narrow slits in the front and rear covers. This way the exposure time of the wafers to UV light is only 12 s.

#### 3.2 Inline thermal oxidation

The second oxidation process investigated in this work was carried out in a commercially available inline furnace supplied by Centrotherm, see Fig. 6. The wafers were heated up by infrared lamps and the only gas supply to the furnace interior was clean compressed air. The originality of the system lies in the fact that the Si wafers are quasicontinuously transported by high-purity ceramic strings. The strings are spanned over the whole length of the furnace and carry the overlying wafers according to the walking-beam principle through the heated muffle as described in detail in [14]. The high purity of the strings together with the fact that they don't move far in the furnace eliminate the contamination of the Si wafers by metallic impurities which is often observed for conventional transport belts made of steel. In our study the speed of the 5-lane transport system was varied between 1 and 3 m/min corresponding to a throughput of up to 5400 cells per hour. The resulting temperature profile measured by built-in thermocouples is shown in Fig. 7. The applied peak temperature was 820°C as it yielded good results in a preliminary test.



Fig. 6: Photo of the IR-heated walking-string furnace.



**Fig. 7:** Temperature profile measured by thermocouples built in the hot zone of the walking-string furnace. The transport speed was 3 m/min.

### 4. **RESULTS**

#### 4.1 PID-s test of UV oxidized cells

3 UV oxidation runs were performed with the same parameters in order to check the process repeatability. 16 cells per run were PID-s stressed and Fig. 8 shows the obtained shunt resistances after the test. It can be seen from the figure, that  $R_{p,after PID}$  is similar for the 3 runs. The median  $R_{p,after PID}$  exceeds 13 k $\Omega$ cm<sup>2</sup> and the minimum  $R_{p,after}$ PID is 4 k $\Omega$ cm<sup>2</sup>. The latter corresponds to a normalised efficiency change of about 1.5%, see Fig. 3. Without UV oxide  $R_{p,after PID}$  was less than 0.2 k $\Omega$ cm<sup>2</sup> and the normalised efficiency change was > 10 %.

The UV oxide thickness was measured by ellipsometry on a polished *p*-type FZ Si reference wafer without  $n^+$ diffusion. The obtained value was about 2 nm. On the  $n^+$ diffused mc Si cells we expect the SiO<sub>2</sub> film to be thicker, but we could not conduct ellipsometry on the textured surface with the desired precision.

It is important to note, that the average efficiency of the cells with UV oxide measured before PID-s was about 0.3% relative lower than the average efficiency of the reference group without UV oxide. The reason is probably a slightly increased front surface recombination velocity. It



**Fig. 8:** Box plot of shunt resistances measured after PID-s solar cell test. The cells feature a UV SiO<sub>2</sub> interlayer. Without SiO<sub>2</sub> interlayer  $R_{p,after PID}$  was < 0.2 k $\Omega$ cm<sup>2</sup>.

might be decreased by applying the SQi technology mentioned in the introduction. Another option is the use of a higher energetic UV radiation provided by an excimer lamp as described e. g. in [15].

#### 4.2 PID-s test of thermally oxidized cells

Fig. 9 shows the measured  $R_{p,after PID}$  of the cells which were oxidized in the walking-string furnace. The cells' PID-s resistance is remarkably high. No correlation of  $R_{p,after PID}$  with the transport speed is visible. The median  $R_{p,after PID}$  exceeds 74 k $\Omega$ cm<sup>2</sup> and the minimum  $R_{p,after PID}$  is 45 k $\Omega$ cm<sup>2</sup>, about one order of magnitude higher than for the UV oxidized cells. The corresponding efficiency degradation is negligible. Obviously, even for the highest speed of 3 m/min the thermal SiO<sub>2</sub> films are thick and dense enough. According to the model for the explanation of PID-s proposed in [3,4] the prepared SiO<sub>2</sub> films seem to be an effective diffusion barrier or trap layer for Na ions.

#### 4.3 PID-s test of modules containing UV oxidized cells

In order to determine the bottom line PID-s module resistance obtained in this work, the less PID-s resistant UV oxidized cells were encapsulated in PV modules. Fig. 10 shows the time course of the electrical module power measured at maximum power point ( $P_{mpp}$ ) during the PID-s test. It can be seen, that  $P_{mpp}$  decreased by less than 0.4% relative after 6 days stress. After 9 days  $P_{mpp}$  of module 1 degraded by 14%,  $P_{mpp}$  of module 2 by 24% relative. Fig. 10 also shows that the reference module, which contained cells without oxide, degraded drastically by 98% after 7 days.

At the end of the test, after 9 days, the modules containing UV oxidized cells were examined by electroluminescence (EL) imaging, see Fig. 11. The EL pictures reveal that only single cells are shorted due to PID-s and turned dark. They limit the measured module power. We assume that the reason is a small variation of the oxide film thickness from cell to cell.

The parameters of the applied accelerated test were quite harsh (85°C and 2000 V with Al foil on top as described before). These test conditions have to be compared with the ones proposed in the new edition of the IEC 62804 standard: 60°C, 85% relative humidity (no conductive layer



**Fig. 9:** Shunt resistances measured after PID-s cell test. The cells feature inline thermal oxide films prepared at 3 different transport speeds.



**Fig. 10:** Measured electrical module power degradation during stress test at 85°C and 2000 V. The cells in modules 1 and 2 feature UV oxide.



**Fig. 11:** Electroluminescence images taken from module 1 (left) and 2 (right) under forward bias after 9 days PID-s.

on the front surface), system voltage stress condition (1000 V in this case) and a maximum allowed PID-s of 5% after 4 days stress time [16]. Because the UV oxide stabilized cells passed the harsher test we conclude that this technology is well suited to meet the upcoming standard. The same holds true for the investigated inline thermal oxidation which lead to even higher PID-s resistance.

#### 5. SUMMARY

We investigated two inline oxidation processes with the aim to stabilize industrial *p*-type multicrystalline Si solar cells against PID-s. The formed SiO<sub>2</sub> layer is located between the  $n^+$ -diffused emitter and the SiN antireflection coating of the cells. The first process, UV oxidation, turned out to yield sufficiently PID-s resistant cells to meet the requirements stated in the new edition of the IEC 62804 standard for design qualification and type approval. An advantage of the technology is the very small footprint of the UV lamp. Hence, it can be retrofitted to virtually every existing cell production line. A drawback is that the cell efficiency measured before PID-s was 0.3% relative lower compared to cells without UV oxide. This might be improved by the SQi technology introduced in [6,7]. The second investigated technology was thermal oxidation in an IR-heated walking-string furnace. The manufactured cells were even more PID-s resistant than the UV oxidized cells. An additional benefit of this process is an increase of the cell efficiency by 0.2% measured before PID-s relative to cells without oxide.

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# REFERENCES

- J. Berghold, O. Frank, H. Hoehne, S. Pingel, B. Richardson and M. Winkler, *Proceedings of the 25<sup>th</sup> European Photovoltaic Solar Energy Conference* (2010) 3753.
- [2] P. Hacke, K. Terwilliger, S. Glick, D. Trudell, N. Bosco, S. Johnston and Sarah Kurtz, *Proceedings of* the 35<sup>th</sup> IEEE Photovoltaic Specialist Conference (2010) 244.
- [3] V. Naumann, D. Lausch, S. Großer, M. Werner, S. Swatek, C. Hagendorf and J. Bagdahn, Energy Procedia 33 (2013) 76.
- [4] V. Naumann, D. Lausch, A. Hähnel, J. Bauer, O. Breitenstein, A. Graff, M. Werner, S. Swatek, J. Bagdahn and C. Hagendorf, Solar Energy Materials & Solar Cells 120 (2014) 383.
- [5] H. Nagel, A. Metz and K. Wangemann, Proceedings of the 26<sup>th</sup> European Photovoltaic Solar Energy Conference (2011) 3107.
- [6] H. Mehlich, D. Decker, U. Scheit, M. Uhlig, S. Frigge, M. Runge, B. Heinze, H.-P. Sperrlich, J. Mai, H. Schlemm, E. Vetter, J. Höhne, S. Reichel, W. Stein, *Proceedings of the 27<sup>th</sup> European Photovoltaic Solar Energy Conference* (2012) 3411.
- [7] http://www.meyerburger.com/en/products-systems/ competences/coating/photovoltaics/industrial-coatingsystems/sqi/
- [8] W. Han, W. Shan, S. Liu, W. Li, X. Niu, J. Jin, C. Lu Ji Li and Q. Zhai, Proceedings of the 28<sup>th</sup> European Photovoltaic Solar Energy Conference (2013) 3309.
- [9] H. Nagel, DE 10 2011 051 112 (2011).
- [10] V. Naumann, D. Lausch, C. Hagendorf and J. Bagdahn, DE 10 2012 022 825 (2012).
- [11] D. Lausch, V. Naumann, O. Breitenstein, J. Bauer, A. Graff, J. Bagdahn and C. Hagendorf, *Proceedings of the 39<sup>th</sup> IEEE Photovoltaic Specialists Conference* (2013).
- [12] www.heraeus-noblelight.com
- [13] I. W. Boyd, Materials Chemistry and Physics 41 (1995) 266.
- [14] D. Biro, R. Preu, O. Schultz, S. Peters, D. M. Huljic, D. Zickermann, R. Schindler, R. Lüdemann and G. Willecke, Solar Energy Materials & Solar Cells 74 (2002) 35.
- [15] A. Moldovan, F. Feldmann, G. Krugel, M. Zimmer, J. Rentsch, M. Hermle, A. Roth-Fölsch, K. Kaufmann and C. Hagendorf, Energy Procedia (2014).
- [16] P. Hacke, R. Smith, K. Terwilliger, G. Perrin, B. Sekulic and S. Kurtz, *Proceedings of the 28<sup>th</sup> European Photovoltaic Solar Energy Conference* (2013) 2944.