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STUDY OF THE ELECTRICAL INSULATION OF DIELECTRIC PASSIVATION LAYERS AND STACKS FOR BACK-CONTACT BACK-JUNCTION SILICON SOLAR CELLS

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ABSTRACT: Within this work an intensive study concerning the electrical insulation of dielectric passivation layers is carried out. Therefore, metal-insulator-semiconductor (MIS) structures are manufactured. By using a 4-point measurement setup with ultra-sensitive piko-ampere meters, shunt resistances of the insulation layers and stacks within these MIS-structures are determined. Most promising is the combination of atomic layer deposited (ALD) aluminum oxide (Al_2O_3) with a thickness of 20 nm and plasma enhanced chemical vapor deposited (PECVD) silicon oxide (SiO_x) with a thickness of 1500 nm. These layers allow for median shunt resistances higher than 30 MΩcm^2 and a complete electrical insulation of wafers with an edge length of 156 mm. It is shown that the layer thickness of both, Al_2O_3 and SiO_x, have a significant impact on the insulation properties of the whole stack. Defects in insulation layers which are short-circuited by the metallization are made visible by infra red (IR) measurements.
Keywords: Devices, electrical properties, passivation.

1 INTRODUCTION

Aiming at industrial solar cell fabrication, the module costs have to be lowered while the power output needs to be increased. This can be done by either decreasing the overall solar cell manufacturing costs including material, process and module costs or by increasing the solar cell efficiency [1]. One very promising approach for decreasing optical losses on the front side of the cell and thus increasing the solar cell efficiency is to electrically contact solar cells only at the rear side of the cell. Hence, the front side can be completely optimized regarding optical and passivation issues. This sophisticated cell-type is the so-called back-contact back-junction (BC-BJ) silicon solar cell, showing already cell efficiencies well above 24% [2]. Since these solar cells integrate bipolar doped areas and contacts on the rear side, shunting problems are crucial [3]. In Figure 1 the schematic cross section of a *n*-type BC-BJ solar cell with and without rear insulation layer is shown.

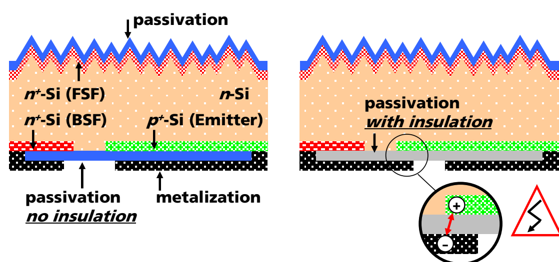

Figure 1: Schematic cross section of a BC-BJ solar cell with (left) and without insulation layer (right). The generation of a shunting current which might occur due to metal fingers (above the BSF) overlapping and contacting the BSF and the gap between BSF and emitter is depicted as well.

BC-BJ cells featuring these insulation layers have several advantages. Since an overlap of the metallization pattern and the *pn*-junction is allowed, metal fingers can be broadened to a size larger than the width of the back surface field (n^+-BSF) or point-like BSF regions can be applied. This is especially advantageous as BC-BJ solar cells need to be scaled to larger wafer formats. The square increase of series resistance losses due to prolonged metal fingers can be balanced by increasing the metallization thickness, but also the width of the metal fingers above the n^+-BSF regions [4]. Since the shape of the *pn*-junction can be decoupled completely from the one of the metal fingers, doping structures with very high emitter coverage are possible. Assuming p^+-passivating thin films like e.g. Al_2O_3 as rear side passivation layer, the higher emitter coverage can lead to both, a high ability for collecting excess carriers as well as very well passivated solar cells. The integration of a point-like back-surface field is possible as well [5] and thus electrical shading losses on the cell rear side can be fully avoided. Finally, thick dielectric layers on the cell rear side lead to a more efficient light trapping [6].

The purposes of this work are defect free insulation layers and stacks that are suitable as rear side passivation and insulation layer in *n*-type BC-BJ solar cells.

2 SAMPLE PREPARATION

2.1 Sample structure and sample preparation

By aiming at the electrical characterization of thin films, a MIS-structure is used within this work. There are many processes within the process flow of a MIS-structure which could influence the defect density in insulation layers. For example, inadequate cleaning before the deposition of insulation layers could lead to the incorporation of dust particles within the layers and hence to a poor adhesion of the layers upon the substrate. Due to dust particles, also the appearance of pinholes during deposition of insulation layers might be favored. Process type and process parameters during the deposition of insulation layers can lead to an amorphous or even porous morphology of the layers. Last but not least, contacting metallization technologies and thermal processes as well can lead to mechanical stress and thus

to a delamination, buckling and spalling of the insulation layers during metallization [7]. Hence, the electrical properties of layers used as insulator in a MIS-structure strongly depend on the process flow. Within this work, the following process flow is focused on.

The MIS-structures were integrated in large scale Czochralski (Cz) *n*-type wafers with an edge to edge length of 156 mm (see Figure 2). After saw damage removal the wafers were cleaned in a standard clean 1 and 2 (SC1-SC2 cleaning). Directly after cleaning, n^+-doping was carried out in a quartz tube furnace, by using the gaseous precursor $POCl_3$. For the removal of the phosphorus-doped silicate glas after diffusion, the diffusion was followed by an etching step in hydrofluoric acid. Afterwards, the insulation layer or respectively the insulation layer stack was deposited on one side of the wafer. For the minimization of any interaction of the layers with the natural laboratory environment, the layers corresponding to a stack were deposited one after the other within one hour. The metallization was carried out directly after the deposition of the insulation layers without cleaning in between, since e.g. an additional HF-Dip would probably lead to a pinhole formation within the insulation layers. Aiming at the formation of metal electrodes, a local etch mask (on the side of the insulator) and a full square etch mask were printed, followed by a selective etching step. The local etch mask design allows for the assembly of 16 MIS-structures with an electrode area of 2 x 2 cm^2. By removing the etch mask in a chemical cascade consisting of acetone and isopropyl, the production of the MIS-structures was finished.

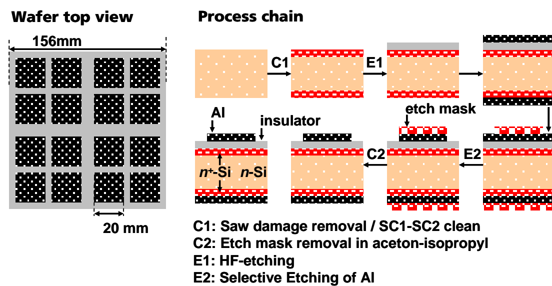

Figure 2: Wafer top view showing the positioning of the several MIS-structures upon a wafer (left) and process chain for the assembly of MIS-structures (right).

2.2 Measurement setup

Aiming at recording of current voltage (*IV*) characteristics of the MIS-structures, a so-called 4-point measurement setup is used (see Figure 3). Therefore, the fully metalized rear side (lower electrode of MIS-structure in Figure 3) of the samples is applied on a metalized table, being connected to a voltage source and an ampere meter. The electrode on the front side of the MIS-structure is connected to a voltage source and an ampere meter as well. Finally a voltage sweep in the range of -2 Volts $< V <$ 2 Volts is carried out, and the current flowing through the MIS-structures from the upper to the lower electrode is measured by two piko-ampere meters. The usage of an ampere meter allowing for the measurement of very small currents is necessary, since a dielectric or respectively insulation layer should generally allow only for the generation of very small currents.

After recording *IV*-characteristics, a determination of the absolute and the relative (infinitesimal) resistance is possible. For a MIS-structure behaving like an ohmic resistor with a linear *IV*-curve, the absolute and the relative resistance are almost identical. MIS-structures integrating a perfect dielectric layer behave non-linearly (hysteresis like) and thus the absolute and the relative resistance differ. To get a quantitative value of the resistance for MIS-structures with non-linear *IV*-characteristics, the absolute resistance corresponding to a current at a defined voltage was determined within this study. Since non-linear MIS-structures are usually realized by perfect insulators, the currents flowing are generated by displacement currents within the dielectric. These currents are very low and correspond to a very high resistance.

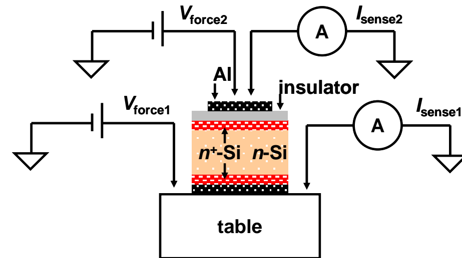

Figure 3: Setup for the *IV*-characterization of MIS-structures. The setup corresponds to a 4-point measurement setup allowing for the application of two electrical potentials (V_{force1} and V_{force2}) and the measurement of current by two piko-ampere meters (I_{sense1} and I_{sense2}).

According to the 2D-model of silicon solar cells, a shunt resistance of 10 k$\Omega$$cm^2$ corresponds to an absolute fill factor loss of 0.2% [8]. In these investigations, the latter absolute fill factor loss is defined as the upper limit. Hence, insulation stacks with a shunt resistance higher than the critical shunt resistance $R_{sh,crit}$ = 10 kΩcm^2 are aimed at.

2.3 Description of experiment

Several MIS-structures were fabricated integrating combinations of thin films to an insulation stack (insulator). As already mentioned the application of insulation stacks for *n*-type BC-BJ solar cells is focused on. These cells feature a rear side with locally doped areas, being heavily doped with phosphorus (n^+-BSF) and boron (p^+-emitter). To reach a high minority collection ability of these cells, the emitter fraction is generally high and hence a high passivation capability of the investigated layers in an insulation layer is of utmost importance. Thus a thin aluminum oxide (Al_2O_3) layer was deposited as a first layer of the insulation stack by means of ALD and PECVD. The following table summarizes the dark saturation current density of silicon surfaces being passivated by Al_2O_3-layers deposited by means of the different techniques.

Table 1: Dark saturation current density J_0 of the Al_2O_3-layers used as first layer of the investigated insulation stacks. The sheet resistances of the boron-doped regions ($R_{sh,p+}$) is given as well.

Material	Technique	$R_{sh,p+}$ (Ω/sq)	J_0 (fA/cm2)	Reference
Al_2O_3	ALD	90	≈ 30	[9]
Al_2O_3	PECVD	90	≈ 36	[10]

Since a sufficient insulation probably can not be reached by a thin Al_2O_3-layer, on these layers a silicon oxide (SiO_x) layer was deposited. Due to technological and optical aspects SiO_x was preferred instead of silicon nitride (SiN_x) films. The SiO_x-layers were deposited by means of PECVD and reactive sputtering.

Table 2: Investigated MIS-structures aiming at the characterization of the technological impact on the electrical properties of insulation stacks.

Insulator		Metallization
Layer1	Layer2	
PECVD-Al_2O_3	PECVD-SiO_x	evaporated Al
ALD-Al_2O_3	PECVD-SiO_x	evaporated Al
ALD-Al_2O_3	PECVD-SiO_x	sputtered Al
ALD-Al_2O_3	Sputtered SiO_x	evaporated Al

In a first experiment, thin layers deposited by means of several technologies were combined to a stack, aiming at the investigation of the so called technological impact on the electrical properties of the insulation stacks. Therefore, the MIS-structures were fabricated with the help of the technologies depicted in Table 2. The layer thicknesses of Al_2O_3 (h_{AlO} = 20 nm) and SiO_x (h_{SiO} = 500 nm) were kept constant for every deposition technology.

Table 3: Investigated MIS-structures integrating insulation stacks of the combination ALD-Al_2O_3 and PECVD-SiO_x. The metallization of the MIS-structures is carried out by evaporation.

layer 1 material	thickness (nm)	layer 2 material	thickness (nm)
ALD-Al_2O_3	20	$PECVD_1$-SiO_x	100
ALD-Al_2O_3	20	$PECVD_1$-SiO_x	500
ALD-Al_2O_3	20	$PECVD_1$-SiO_x	1500
ALD-Al_2O_3	20		
ALD-Al_2O_3	200		
		$PECVD_1$-SiO_x	1500
		$PECVD_2$-SiO_x	1500

$PECVD_i$ PECVD process i

In a second experiment, the electrical properties of ALD-Al_2O_3 and PECVD-SiO_x as insulation stack are evaluated. Unfortunately, thick ALD-Al_2O_3 layers need to be avoided, since the deposition rates of these processes are low compared to other technologies and hence the deposition processes would lead to long deposition and respectively process times [11]. Hence, within this experiment thin ALD-Al_2O_3 (h_{AlO} = 20 nm) layers were deposited and coated by PECVD-SiO_x with a thickness of 100, 500 and 1500 nm. For the realization of the thick SiO_x-layer (h_{SiO}=1500nm), the SiO_x-process leading to a thickness of 500nm was repeated three times. To see if the electrical insulation can either be attributed to the thin Al_2O_3-layer or to the thick SiO_x layer, MIS-structures featuring one single Al_2O_3-layer with a thickness of 20nm and one single SiO_x-layer with a thickness of 1500 were fabricated as references. To investigate the influence of the process setup and the process parameters on the electrical properties of SiO_x-layers, the deposition of the thick SiO_x-layer was also performed with a different PECVD-setup. Aiming at the investigation of the insulating properties of an uncapped Al_2O_3-layer especially in combination with an Al-metallization, also a MIS-structure featuring Al_2O_3 with a thickness of 200 nm was fabricated. The metallization of the MIS-structures was carried out by evaporation.

For the second experiment, the *IV*-characterization was performed before and after a forming gas anneal (FGA). Hence, also the impact of the solar cell specific thermal treatment after metallization on the electrical properties of the insulation stacks is detectable.

In the following the following nomenclature was used: layer1-xx/layer2-yy means an insulation stack consisting of ‘layer1’ with a thickness h_{layer1} = ’xx’ nm and ‘layer2’ with a thickness of h_{layer2} = ’yy’ nm.

3 TECHNOLOGICAL IMPACT

The insulation characteristics of the investigated insulation stacks are summarized in Table 4. Therefore, the median shunt resistance $R_{sh,median}$ as well as the percentage of MIS-structures $f_{R,>10k}$ exceeding the critical shunt resistance $R_{sh,crit}$ are depicted.

Table 4: Median shunt resistance $R_{sh,median}$ of MIS-structures in dependence of the different deposition technologies. The percentage of samples $f_{R>10k}$ featuring shunt resistances exceeding the critical value $R_{sh,crit}$ are shown as well.

MIS-structure	$R_{sh,median}$ (Ωcm^2)	$f_{R>10k}$ (%)
PECVD-Al_2O_3 / PECVD-SiO_x evaporated Al	2.3M	55
ALD-Al_2O_3 / PECVD-SiO_x evaporated Al	36.5M	88
ALD-Al_2O_3 / PECVD-SiO_x sputtered Al	3.1M	56
ALD-Al_2O_3 / sputtered SiO_x evaporated Al	2.2M	69

By comparing the different insulation stacks with evaporated Al, the layer combination of ALD-Al_2O_3 and PECVD-SiO_x has the highest $R_{sh,median}$-value and also the highest percentage of samples being insulating. Unfortunately the electrical properties are not sufficient for the integration in BC-BJ solar cells and also the application of a sputtered metallization has a negative impact on the insulation quality of the insulation stack. The negative influence of the sputtered metallization is probably caused by accelerated inert ions, damaging the insulation layers. Radioactive radiation might be a probable cause for the decreased insulation quality as well. Since insulation stacks including ALD-Al_2O_3 and PECVD-SiO_x show the highest electrical insulation, these stacks are focused on in the second experiment.

4 INSULATION STACK ALD-Al_2O_3 / PECVD-SiO_x

Figure 4 shows the shunt resistance of the several MIS-structures in dependence of the Al_2O_3-layer thickness h_{AlO} and of the SiO_x-layer thickness h_{SiO} before FGA. The R_{sh}-values are plotted as data points as well as box-plots. The $R_{sh,crit}$-value is depicted as solid horizontal line as well. For every insulation layer the percentage of

samples featuring R_{sh}-values exceeding the $R_{sh,crit}$-value before FGA $f_{R>10k}$ and after FGA $f_{R>10k,FGA}$ are depicted along the upper x-Axes.

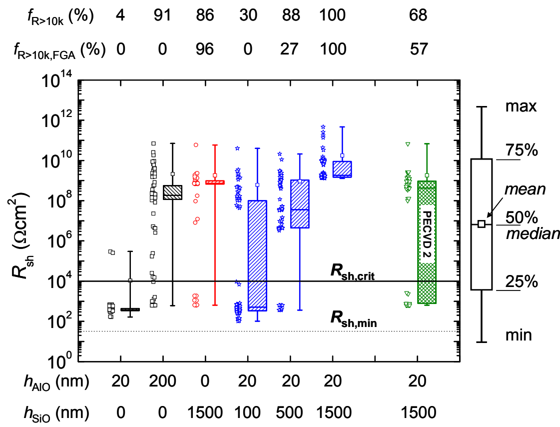

Figure 4: Shunt resistance R_{sh} in dependence of stacks consisting of ALD-Al_2O_3 layers and PECVD-SiO_x layer with different layer thicknesses.

It is clearly visible that the Al_2O_3-20, but also the Al_2O_3-200 layer exhibit no sufficient electrical insulation to be used as insulation layer. For the Al_2O_3-20 layer, the percentage of MIS-structures having an R_{sh} higher $R_{sh,crit}$ is zero before and after FGA. Thicker Al_2O_3 (Al_2O_3-200) feature an $f_{R>10k}$-value of 91% before FGA, but unfortunately this value decreases to zero after FGA as well. These low R_{sh}-values of MIS-structures featuring uncapped Al_2O_3 are probably mainly due to chemical reactions of the Al_2O_3 and the overlaying Al during FGA. The shunt resistances measured on MIS-structures with a thick SiO_x-1500 layer are high and stable during FGA ($f_{R>10k,FGA} = 96\%$). But, a complete electrical insulation is still not reached by the single layer. Comparing the MIS-structures featuring ALD- Al_2O_3 and PECVD-SiO_x with varying h_{SiO}, the insulation quality of the stack increases with increasing thickness. Before FGA, MIS-structures featuring the Al_2O_3-20/SiO_x-100 layer allow for a $f_{R>10k}$ of 27 %. Integrating an Al_2O_3-20/SiO_x-500 layer, this value increases to 84 %. Unfortunately, the insulation quality of both stacks is not stable during FGA. Only the stack Al_2O_3-20/SiO_x-1500 is insulating for every single test sample before and after FGA. The perfect insulation characteristics of the Al_2O_3-20/SiO_x-1500 stack are probably caused by several reasons. Firstly, after ALD of Al_2O_3 the silicon surface and corresponding defects are buried by an almost defect free and homogeneous Al_2O_3-layer. Hence the growth of defects due to surface defects during PECVD might be limited. Secondly, due to the high thickness and the corresponding long deposition times, growing defects like pinholes get thinner and finally pinched off. Thirdly, the deposition of three independent SiO_x-layers (each 500 nm thick) on top of each other might lead to a so-called stuffing of open defects. Unfortunately, the results of the Al_2O_3-20/SiO_x-1500 can not be reproduced, by performing the SiO_x-deposition with a different PECVD-setup (PECVD 2). Hence, the insulation properties of the investigated insulation stack depend strongly on the process and tool setup and the process parameters.

In Figure 5 the R_{sh} of all the measured MIS-structures after FGA (16 MIS-structures per wafer on three wafers) are depicted in a spatially resolved manner. The R_{sh}-values are rated in 'low', 'middle' and 'high' values. 'High' R_{sh}-values mean that the insulating properties of the insulation stack are sufficient to be integrated in a BC-BJ solar cell. In the case of Al_2O_3-20/SiO_x-500 13 out of 46 MIS-structures are 'highly' insulating. Since there are no MIS-structures rated with 'middle' insulating, it seems that insulation stacks often have either defects which are short circuited by the metallization ('low' R_{sh}-values) or the insulation has almost no defects which are short circuited ('high' R_{sh}-values). In the case of the Al_2O_3-20/SiO_x-1500 stack all the analyzed MIS-structures on three different wafers are 'highly' insulating and hence ideal conditions for the integration of this stack in BC-BJ solar cells are given.

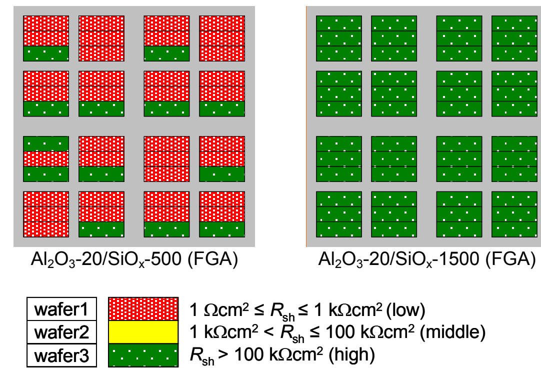

Figure 5: Shunt resistance of several MIS-structures in dependence of the wafer position. A stack consisting of Al_2O_3 with a thickness of 20 nm and SiO_x with a thickness of 500 nm (left) is compared with the same stack featuring a SiO_x with a thickness of 1500nm (right).

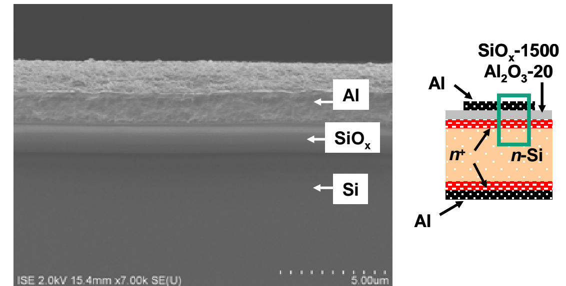

Figure 6: SEM-image of the highly insulating stack Al_2O_3-20/SiO_x-1500 on the left side and a schematic cross section of the SEM-sample on the right side.

Figure 6 shows the magnified cross-section of a MIS-structure featuring the insulating stack Al_2O_3-20/SiO_x-1500 recorded by scanning electron microscopy (SEM). It is clearly visible that the SiO_x-layer is homogeneously deposited. Else, there are no defects visible like e.g. Al-spikes penetrating through the insulation layer. The sandwich-like configuration of the three independently deposited SiO_x-layers is visible as well. It is worth mentioning that the SEM-picture covers only a lateral distance of approximately 25 µm of the MIS-structure cross section. Nevertheless, superior shunting of the Al-layer through the Al_2O_3-20/SiO_x-1500 stack could not be detected by SEM-imaging along the whole 20 mm long cross section of the sample.

6 VISUALIZATION OF DEFECTS

In order to visualize defects within insulation stacks, the infra red (IR) emission of MIS-structures with and without insulation stack was measured by applying a pulsed voltage. The results of these thermographical measurements are depicted in Figure 7. For the MIS-structure without proper insulation, so-called hot spots in the range of the activated area are clearly visible. These hot spots are interpreted as being induced by current flowing through short circuited defects (e.g. pinholes) in the dielectric layer. The increased local heat finally leads to a local IR-emission which can be detected by the IR-detector. These hot-spots already occur for low voltages. For the MIS-structure with highly resistive insulation, no hot-spots are detectable in the range of the activated area. Hence, short circuiting of the insulation layer can probably be neglected. A detectable IR-emission occurs in the surrounding of the activated area, but only for higher voltages.

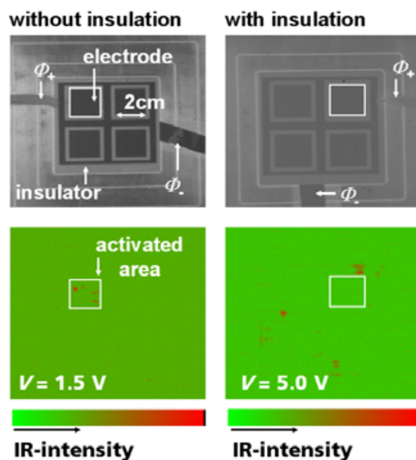

Figure 7: IR images of MIS-structures with (left) and without insulation layers (right). The upper figures show a photograph of the samples during IR-measurement. The lower figures show the spatial-resolved IR-intensity measured by the IR-detector while a voltage is applied. Φ_+ and Φ_- are the potentials of the electrical contacts used for the application of the voltage *V*.

7 CONCLUSIONS AND OUTLOOK

Within this work, insulation stacks for the integration in BC-BJ solar cells were investigated. Insulation stacks combining ALD-Al_2O_3 (h_{AlO} = 20 nm) and PECVD-SiO_x (h_{SiO} = 1500 nm) were found out to have the highest insulation quality. Insulation stacks of this type allow for the complete insulation of several wafers with an edge to edge length of 156 mm. Thus, aiming at up-scaling of the BC-BJ cell format, these insulation stacks are very suitable. In generally, it was found out, that the investigation of insulating thin layers is a challenging issue. These layers incorporate defects on the one hand and the layer properties depend strongly on the process environment (deposition technology, setup, parameters, and metallization technology) on the other. Besides the development of insulation stacks, also characterizing methods were investigated. Thermo graphical measurements using a pulsed voltage and IR-sensitive detectors, allow for the visual detection of defects within the insulation layers. Further studies will focus on a thickness reduction of the ALD-Al_2O_3/PECVD-SiO_x stack, by increasing the Al_2O_3-thickness and decreasing the SiO_x-thickness. Cell adequate insulation stacks will be further evaluated on BC-BJ cell level. Also the characterization of printable thick layers will be focused on.

8 ACKNOWLEDGEMENTS

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