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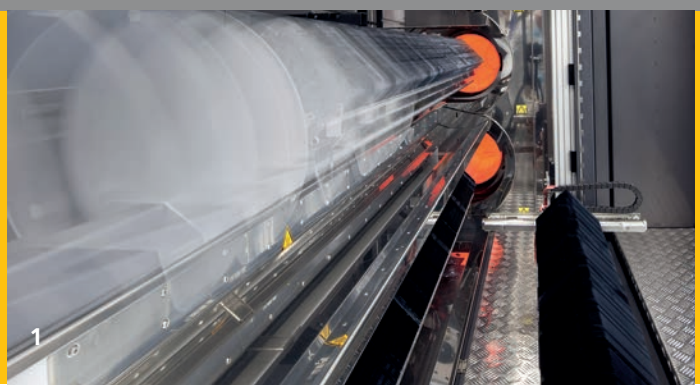
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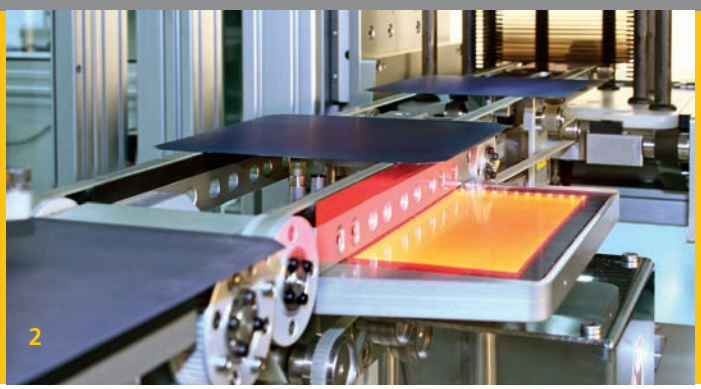
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1 *High capacity oxidation furnace in the Photovoltaic Technology Evaluation Center (PV-TEC).*
2 *Inline quality control of wafers after high-temperature processing.*

THERMAL OXIDE PASSIVATED SOLAR CELLS

Methods for the fabrication of high-quality silicon surface passivation layers have received much attention recently. One approach that makes use of these layers is the Passivated Emitter and Rear Cell (PERC). Compared to conventional solar cells with a full area aluminium alloyed rear contact, the combination of surface passivation layers and local rear contacts results in an improved light trapping and a reduced surface recombination, leading to higher conversion efficiencies.

Passivation layers fabricated by thermal oxidation allow for very low surface recombination velocities on both p- and n-type silicon. These thermal oxide layers can be grown in industrial high-capacity quartz tube furnaces, known from $POCl_3$ diffusion processes. The use of thin thermal oxide layers enables a short cycle time and low process cost of ownership.

For PERC devices fabricated of p-type silicon, thermal oxidation can be implemented into the process sequence in a very cost-effective manner, if it is used for simultaneously growing a high-quality passivation layer for the n-doped emitter and the p-type base at the rear side of the sample. These thermal oxide passivated solar cells feature an increased blue and red response compared to conventional solar cells with aluminium back surface field (Al-BSF) and a single SiN_x antireflection layer. In addition, the thin thermal oxide layer prevents potential-induced degradation (PID).

We have developed a lean process for the industrial fabrication of high-efficiency solar cells, in which a thermal oxide passivates all sides (TOPAS). The process sequence omits the use of masking steps. Instead, inline etching processes are applied to condition the rear surface prior to thermal oxidation.

Established single step screen printing technology forms the front and rear contacts. With this approach, we have achieved conversion efficiencies up to 20.0% for solar cells with an edge length of 156 mm.

Fraunhofer Institute for Solar Energy Systems
Heidenhofstrasse 2
79110 Freiburg
Germany
Phone +49 761 4588-0
Fax +49 761 4588-9000
www.ise.fraunhofer.de

Dr Andreas Wolf
Phone +49 761 4588-5580
andreas.wolf@ise.fraunhofer.de

Dr Ing. Daniel Biro
Phone +49 761 4588-5246
daniel.biro@ise.fraunhofer.de

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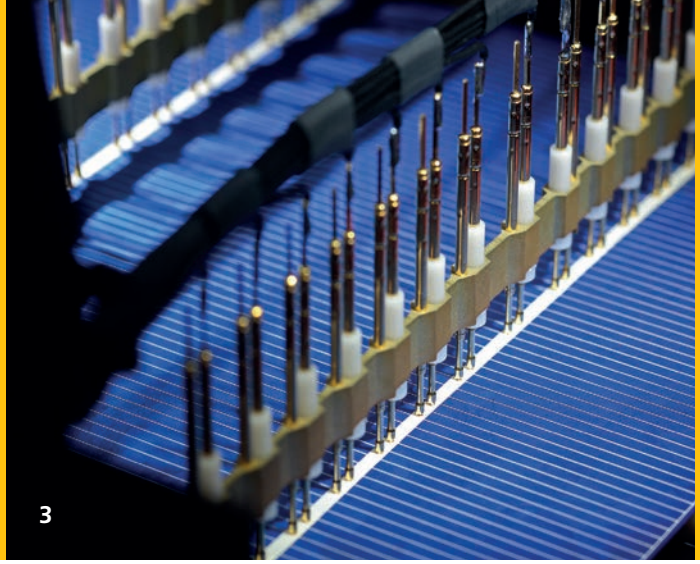

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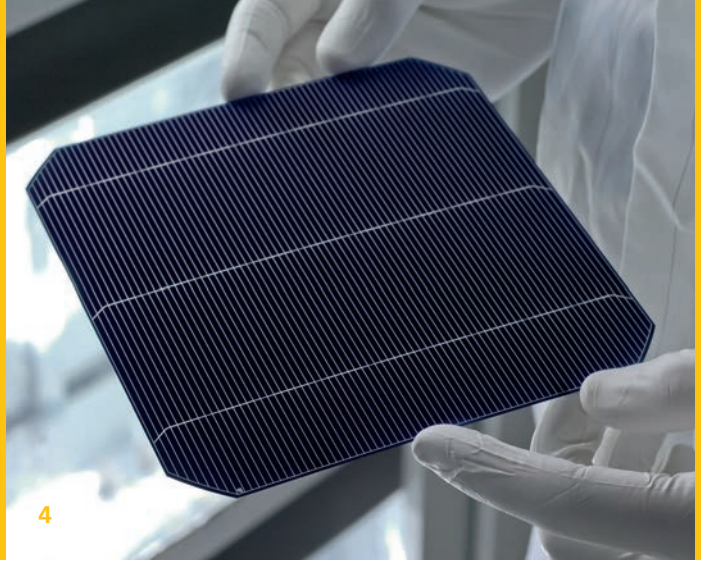

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Application to HIP-MWT Solar Cells

As the use of thermal oxidation is not limited to conventional H-pattern grid devices, we have adapted the process sequence to allow for the implementation of metal-wrap through (MWT) structures. Only one additional process, the drilling of vias, makes the full benefit of reduced shading accessible.

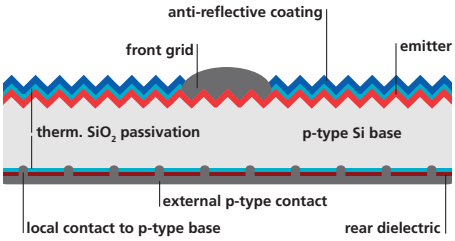
These high-performance MWT (HIP-MWT) solar cells are fabricated with a streamlined process sequence, which allows for conversion efficiencies exceeding 20% (edge length of 156 mm). All solar cells feature screen-printed contacts as well as solder areas and are fully solderable. The alternative use of dispensed Ag front contacts enables conversion efficiencies of 20.6% on FZ-Si wafers with an edge length of 125 mm.

As all solder contacts are located at the rear side, this allows for a potentially simplified interconnection. In addition, the use of thicker interconnectors and an increased packing density results in reduced cell to module losses compared to H-pattern grid cells.

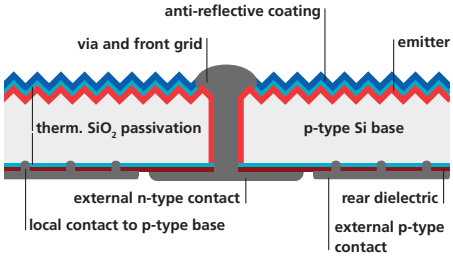
If you plan to increase conversion efficiencies of solar cells with high-quality silicon surface passivation layers, we are happy to support you.

3 *Cell tester measurement of industrial PERC devices.*

4 *HIP-MWT solar cell with passivated rear side and laser fired contacts.*



Schematic cross section of a PERC solar cell with local rear contacts. A thin thermal oxide passivates both front emitter and rear base of the device.



Schematic cross section of a High-Performance MWT (HIP-MWT) solar cell. Minor adaptations of the TOPAS process sequence make the full benefit of reduced shading of the MWT structure accessible.

Si wafer	V_{oc} (mV)	J_{sc} (mA/cm²)	FF (%)	η (%)
mc	630	36.2	77.9	17.7
cast-mono	654	39.0	77.6	19.8*
Cz (B)	649	39.1	77.5	19.7*
Cz (Ga)	655	39.0	78.0	19.9*
magn. Cz (B)	**659**	**38.5**	**78.9**	**20.0***

IV parameters of TOPAS solar cells with an edge length of 156 mm (calibrated measurement at Fraunhofer ISE CalLab PV-Cells, fully solderable).*

Si wafer	V_{oc} (mV)	J_{sc} (mA/cm²)	FF (%)	η (%)
Cz (B)	**664**	**39.2**	**78.1**	**20.3***
	650	39.3	76.7	19.6*
Cz (Ga)	659	39.4	77.1	20.0
magn. Cz (B)	657	39.5	77.7	20.2*

IV parameters of fully solderable HIP-MWT solar cells with thermal oxide passivated surfaces. The edge length is 156 mm (calibrated measurement at Fraunhofer ISE CalLab PV-Cells).*